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APR 1 8 2005
PATENT & TRADEMARK OFFICE

FIG. 1

PRIOR ART

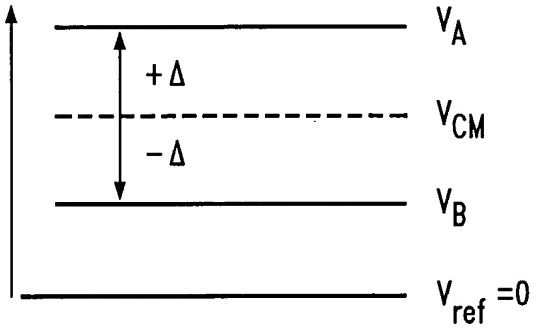
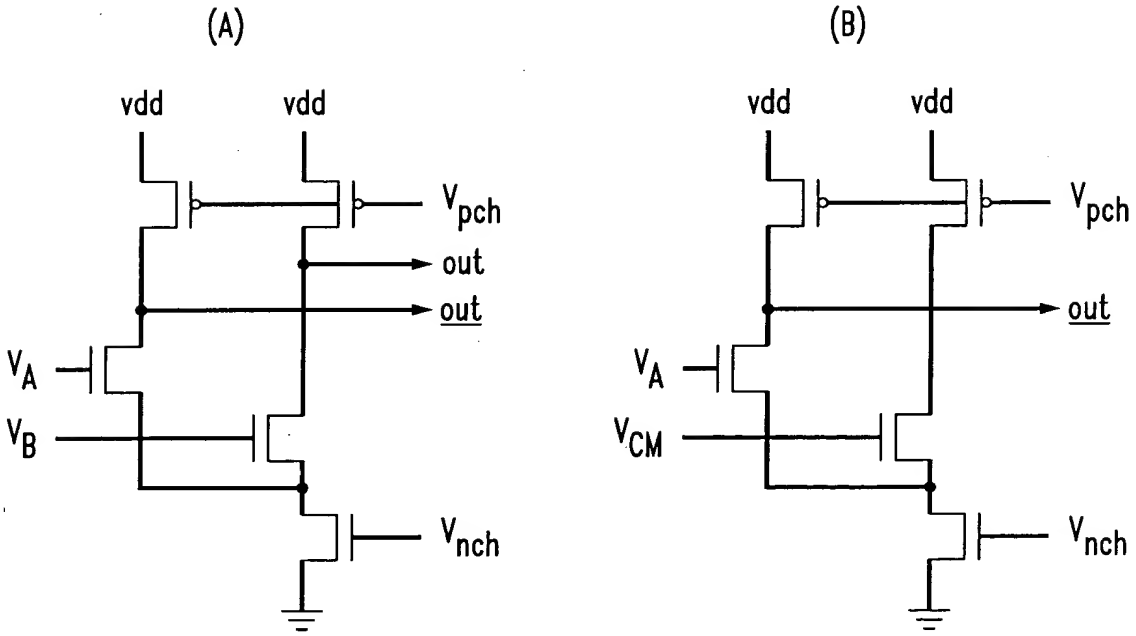


FIG. 2

PRIOR ART



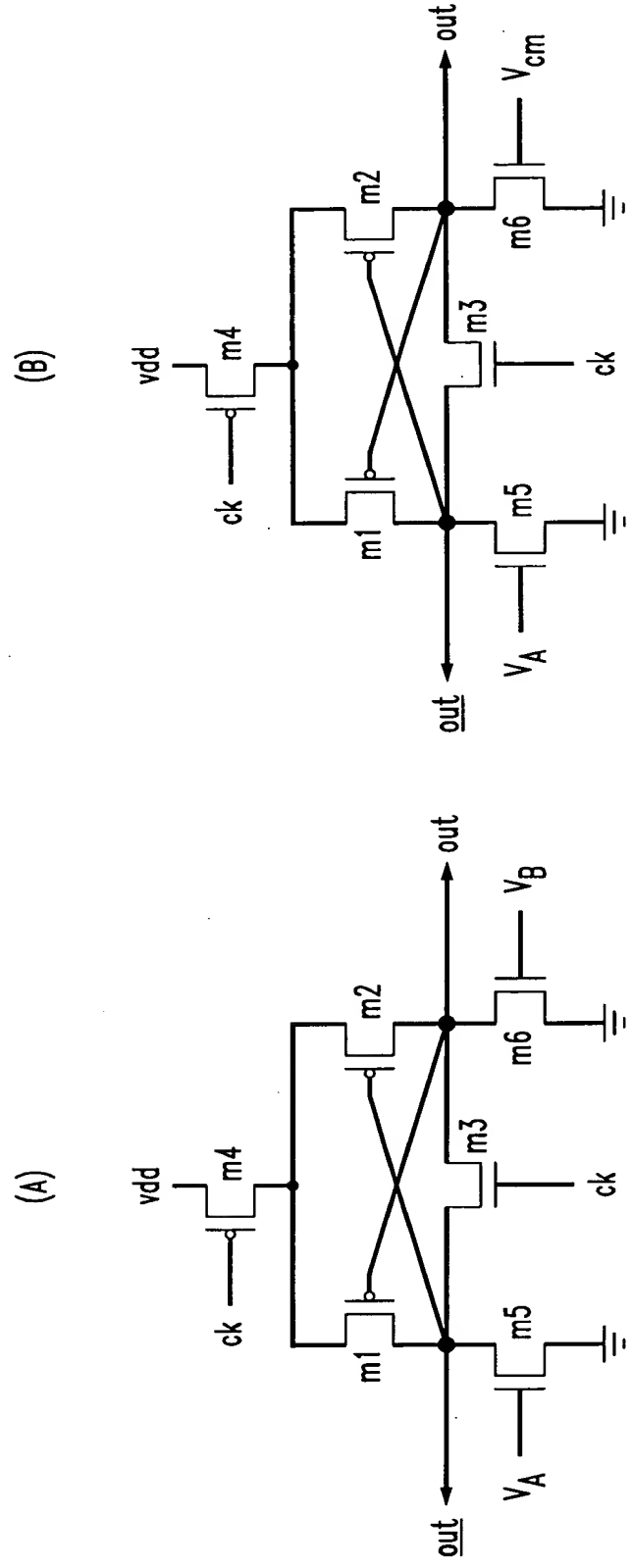


FIG. 3
PRIOR ART

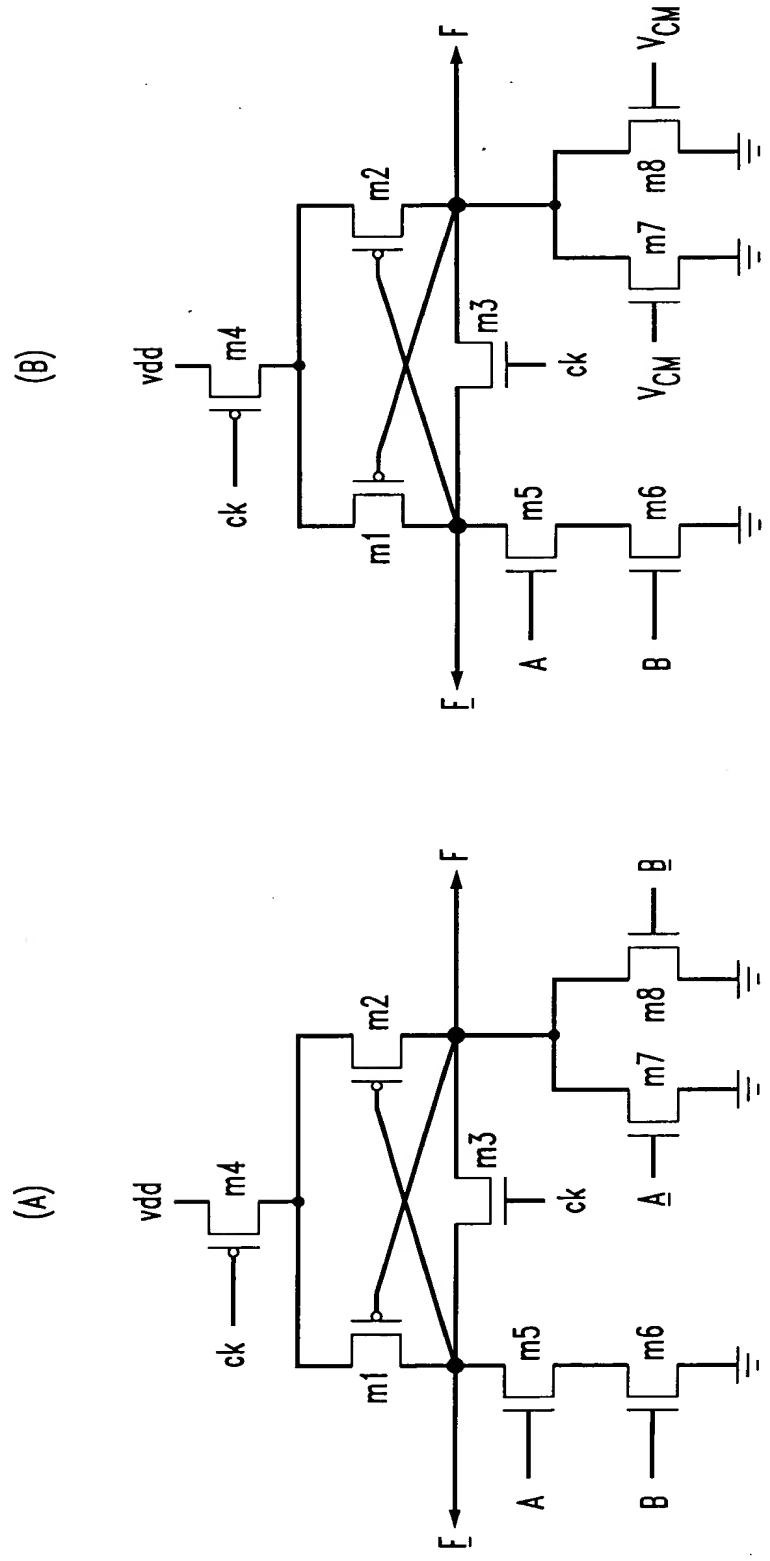


FIG. 4
PRIOR ART

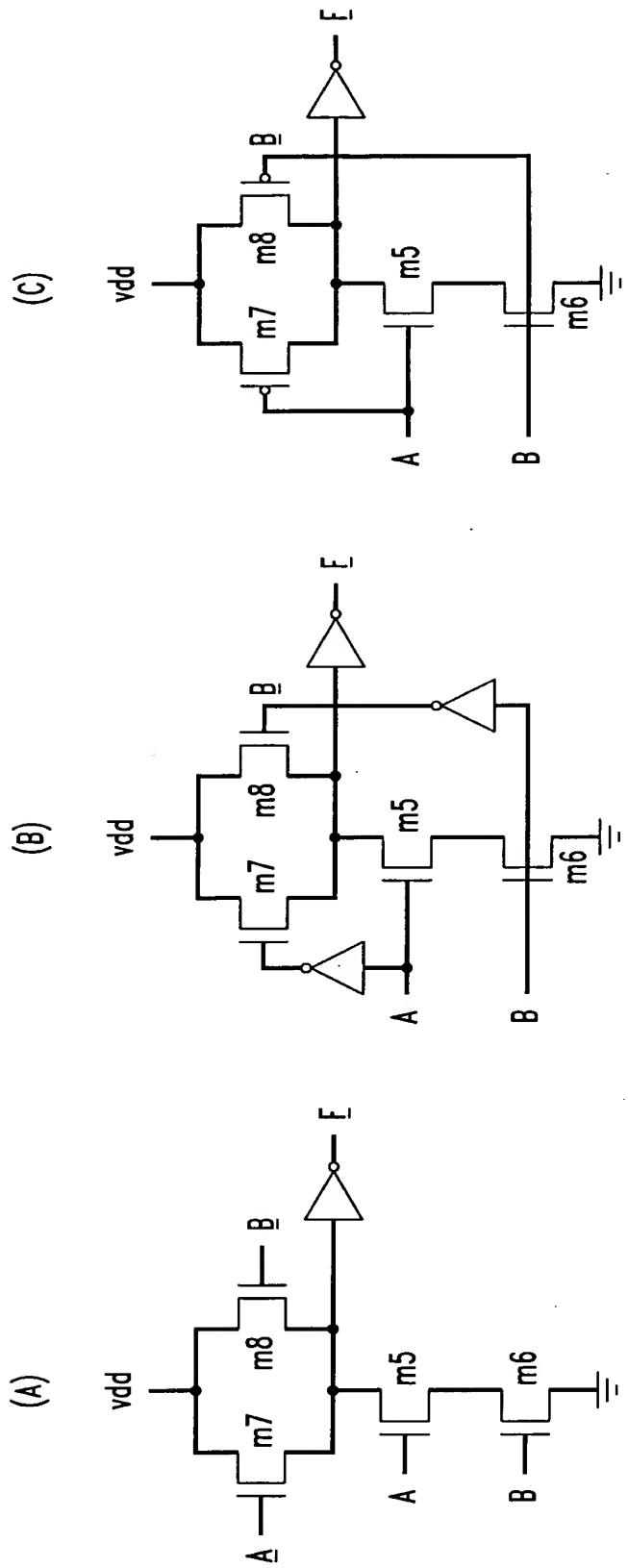


FIG. 5
PRIOR ART

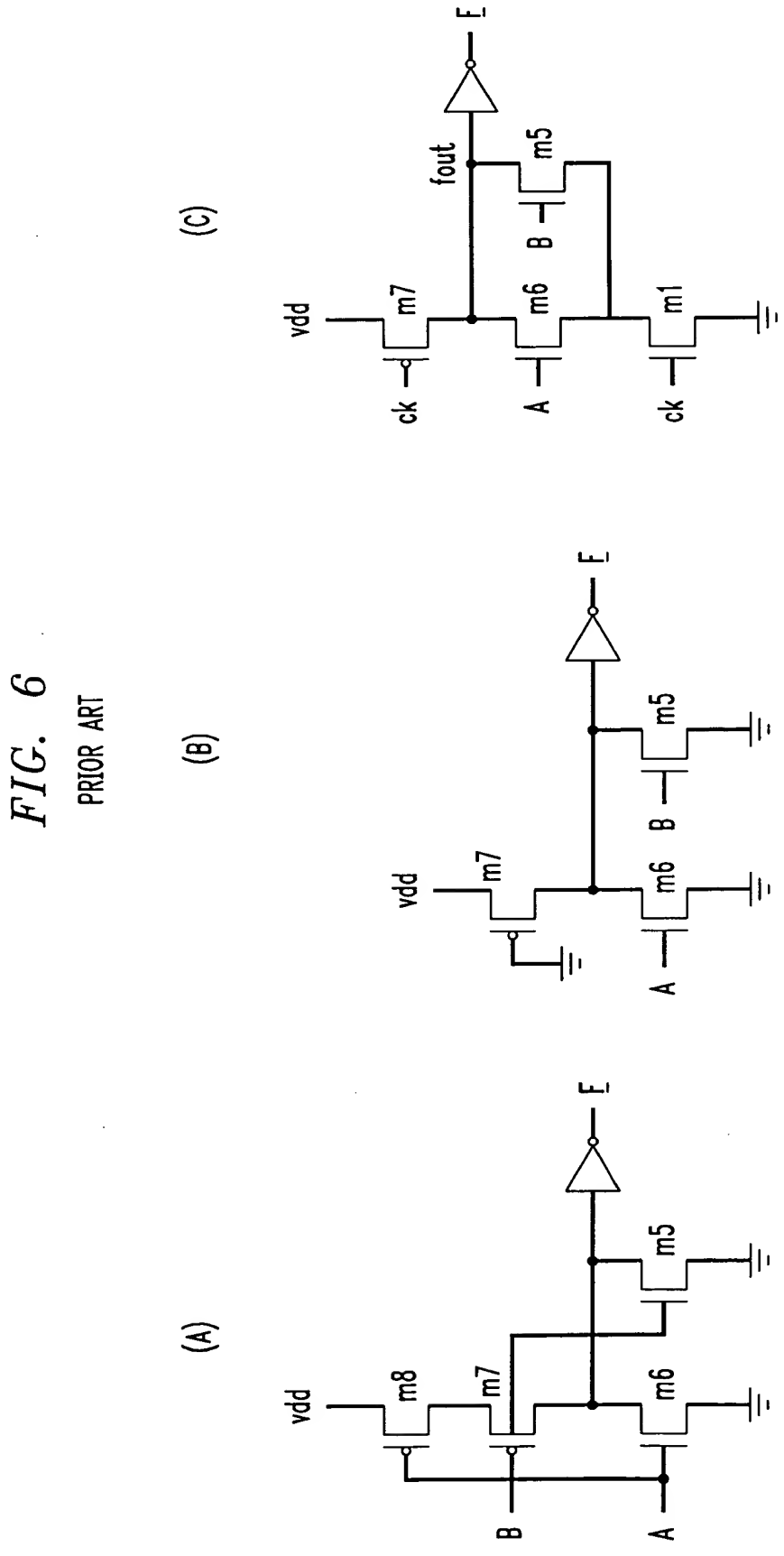


FIG. 6
PRIOR ART

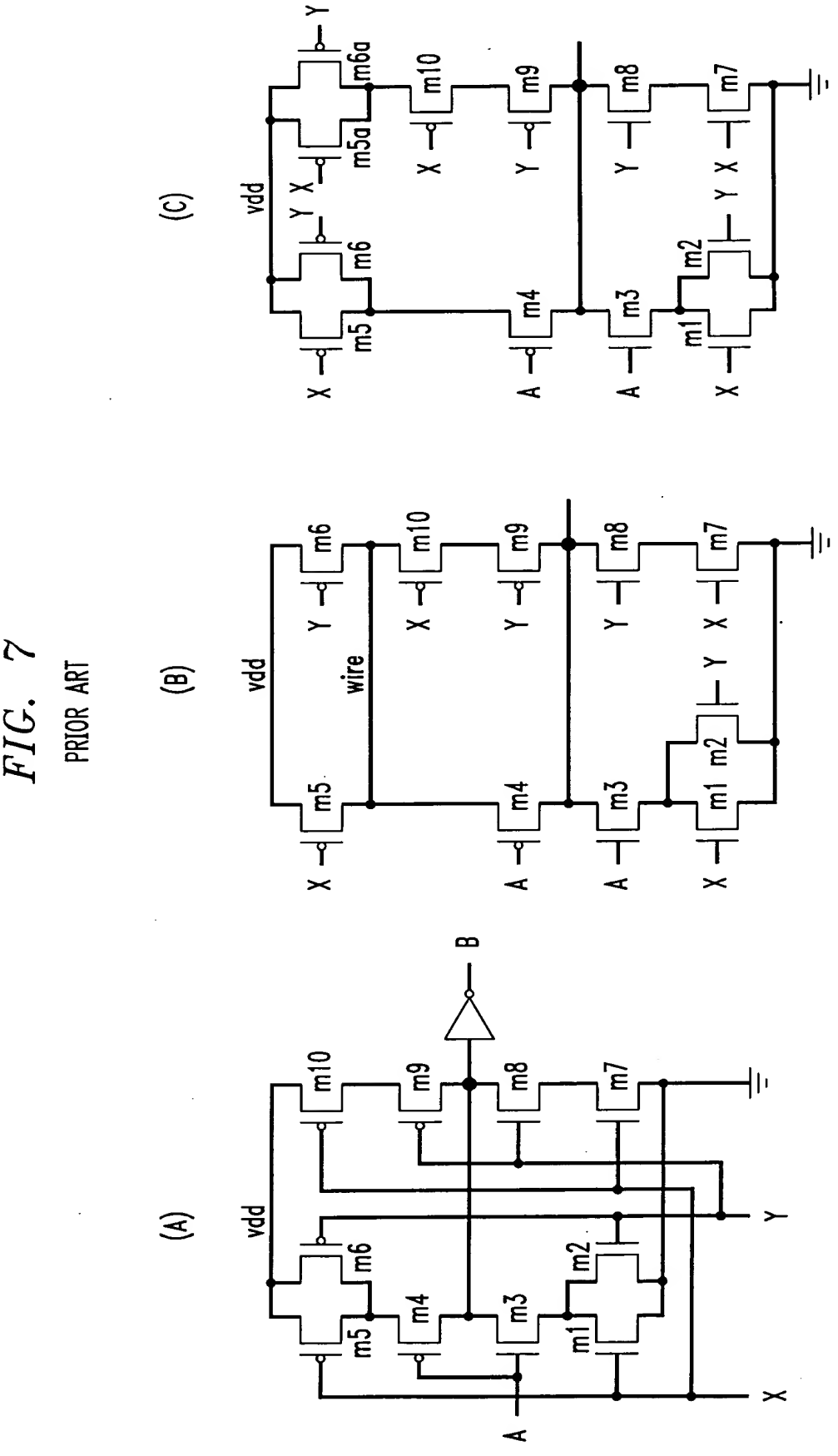


FIG. 7
PRIOR ART

FIG. 8

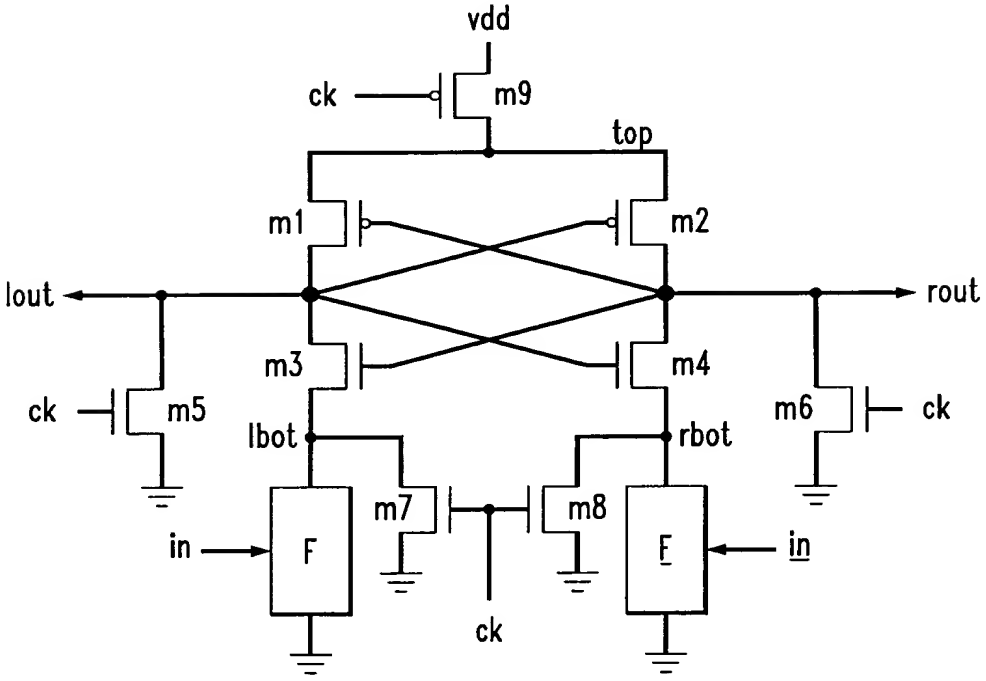

vdd
ck
m9
top
m1
m2
lout
rout
m3
m4
ck
m5
lbot
rbot
m6
ck
m7
m8
in
F
F
in
ck

FIG. 9

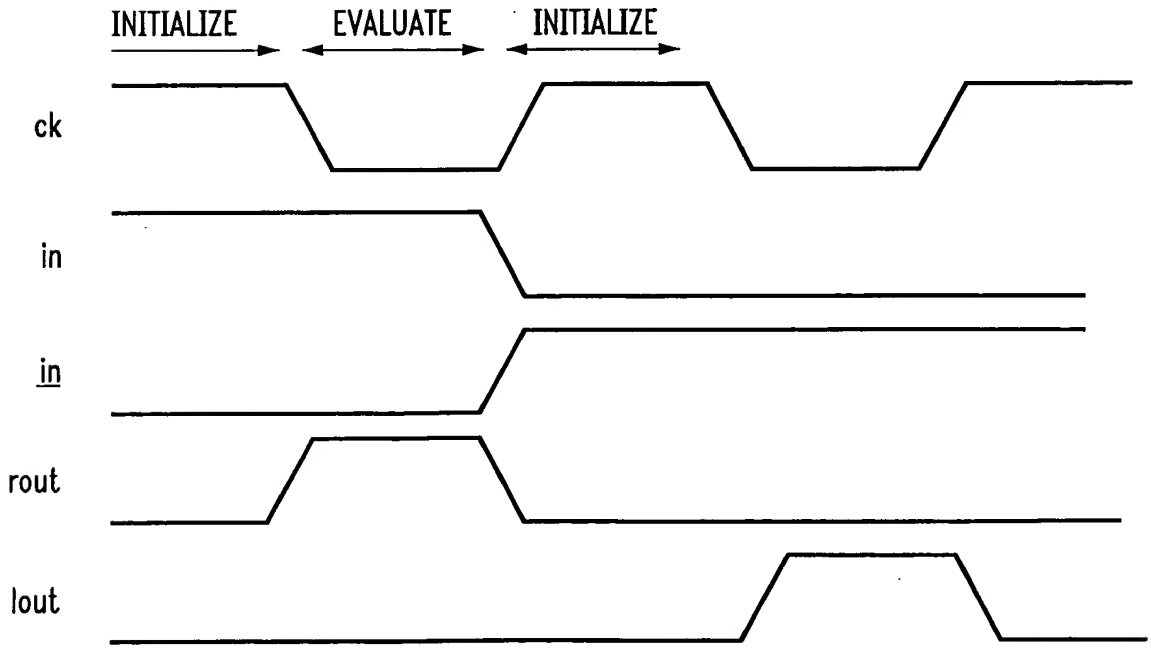

INITIALIZE
EVALUATE
INITIALIZE
ck
in
in
rout
lout

FIG. 10A

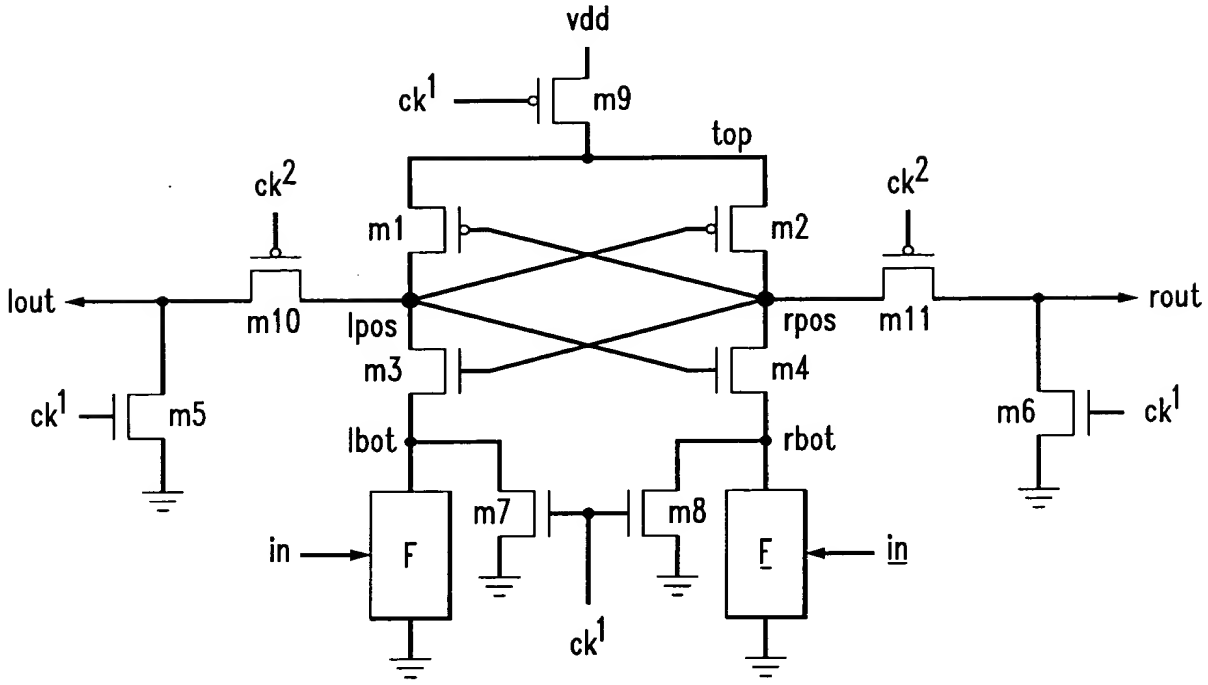


FIG. 10B

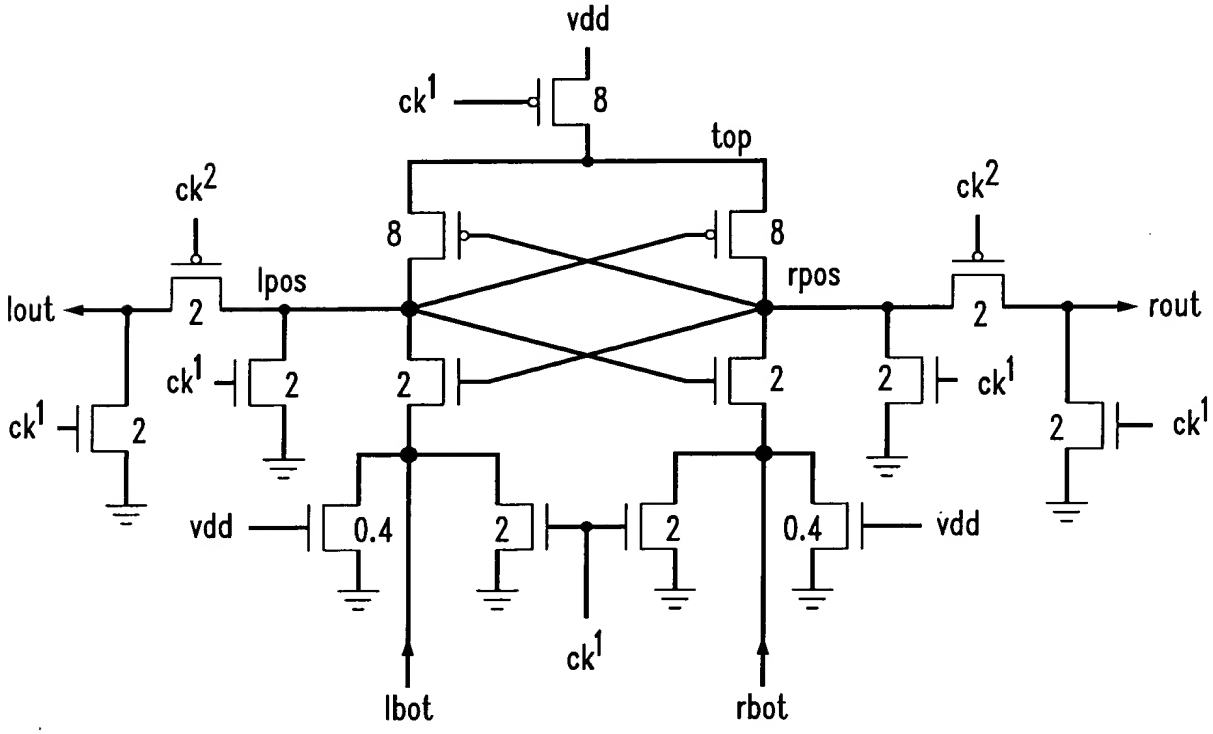
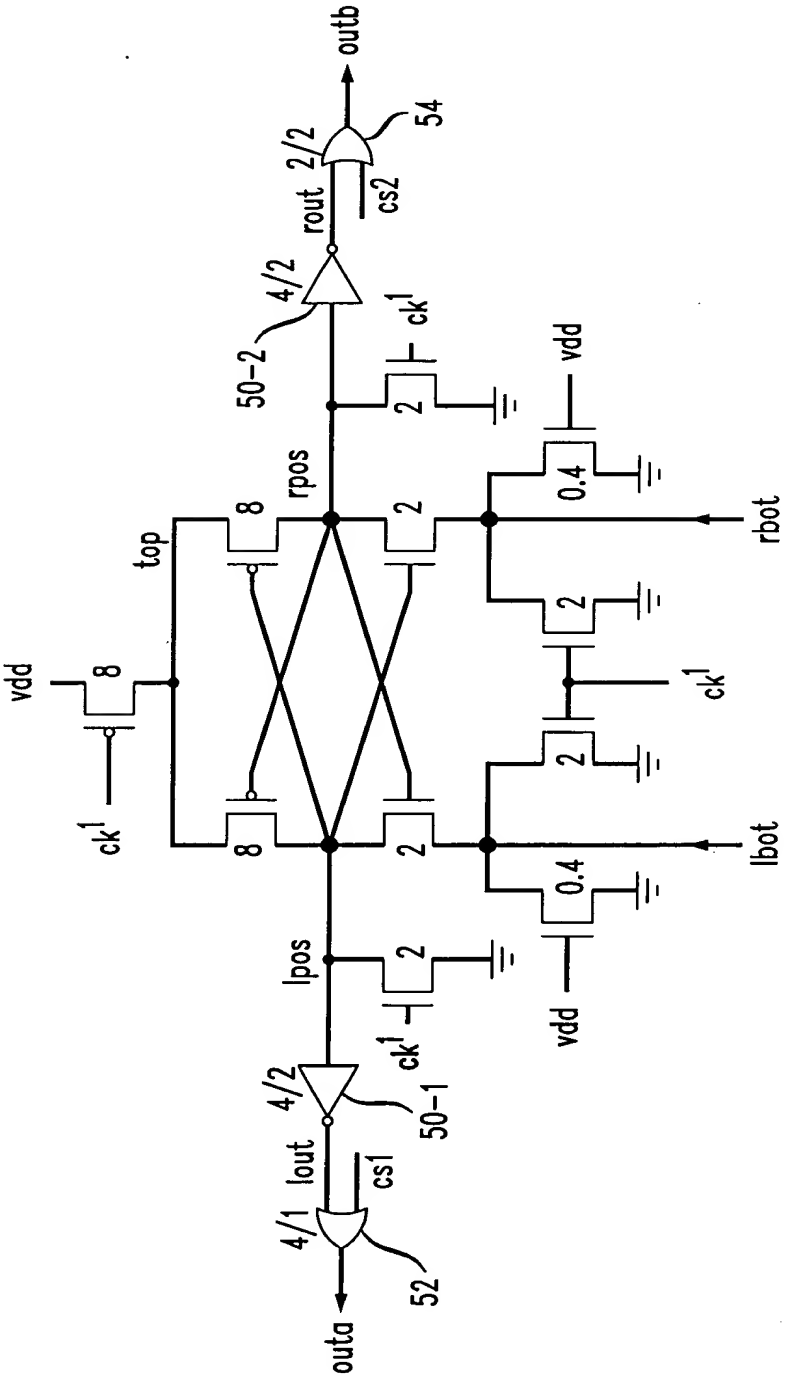


FIG. 10C


outb
54
2/2
rout
cs2
4/2
50-2
ck1
2
vdd
0.4
rpos
8
2
top
rbot
vdd
8
ck1
2
ck1
8
2
0.4
lbot
lpos
2
ck1
vdd
4/2
50-1
lout
cs1
4/1
52
outa

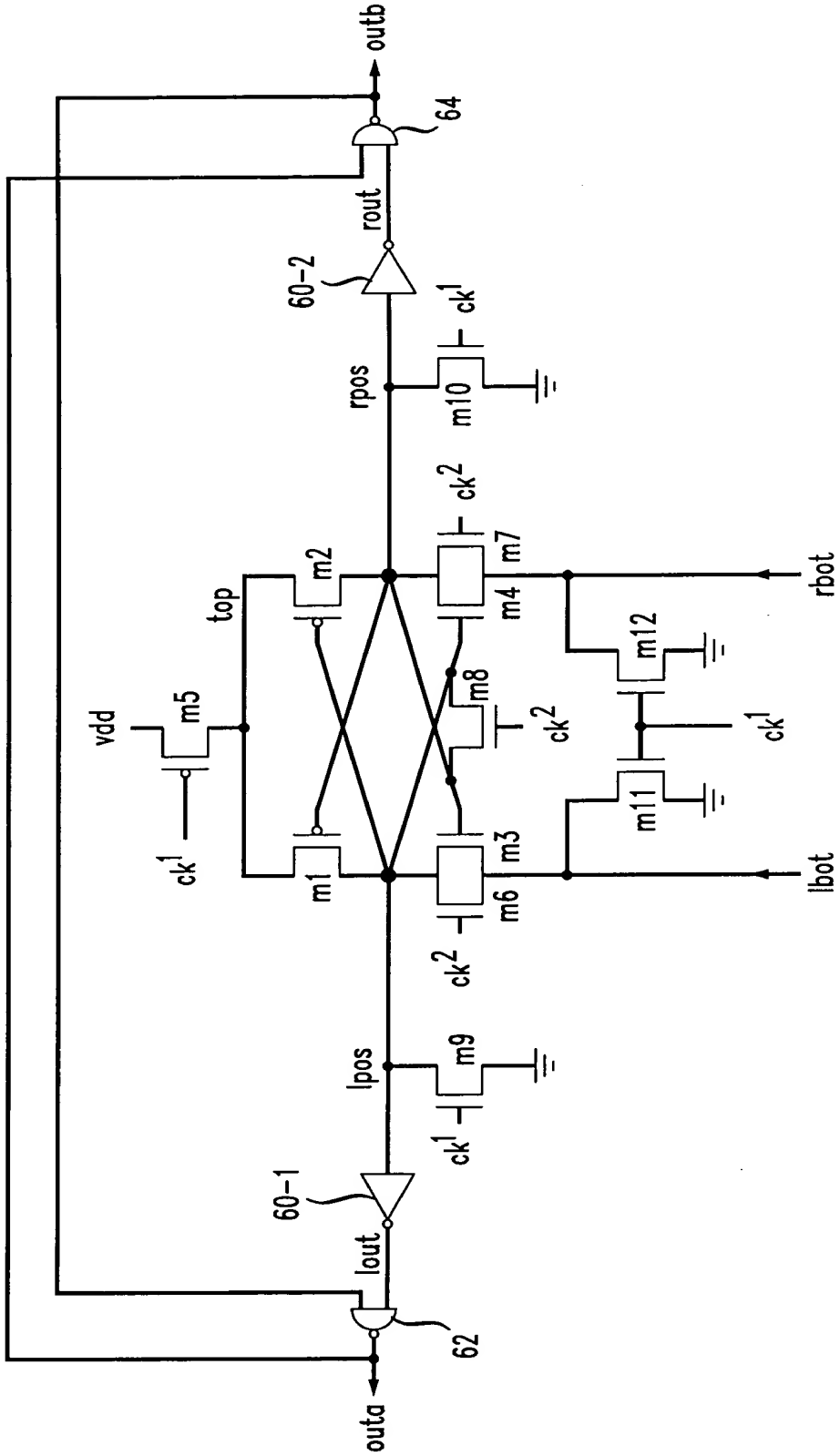

outb
64
rout
60-2
ck1
rpos
m10
ck2
m2
m7
top
m4
rbot
m12
vdd
m5
m8
ck2
ck1
m11
ck1
m1
m3
lbot
m6
ck2
lpos
m9
ck1
60-1
lout
62
outa

FIG. 10D

FIG. 11

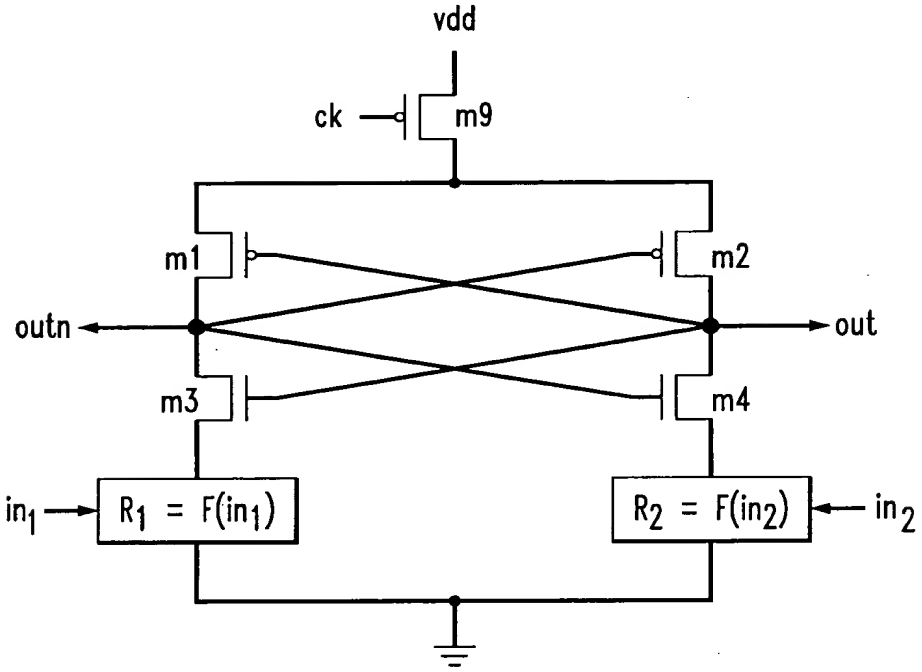

vdd
ck
m9
m1
m2
outn
out
m3
m4
in1
R1 = F(in1)
R2 = F(in2)
in2

FIG. 12

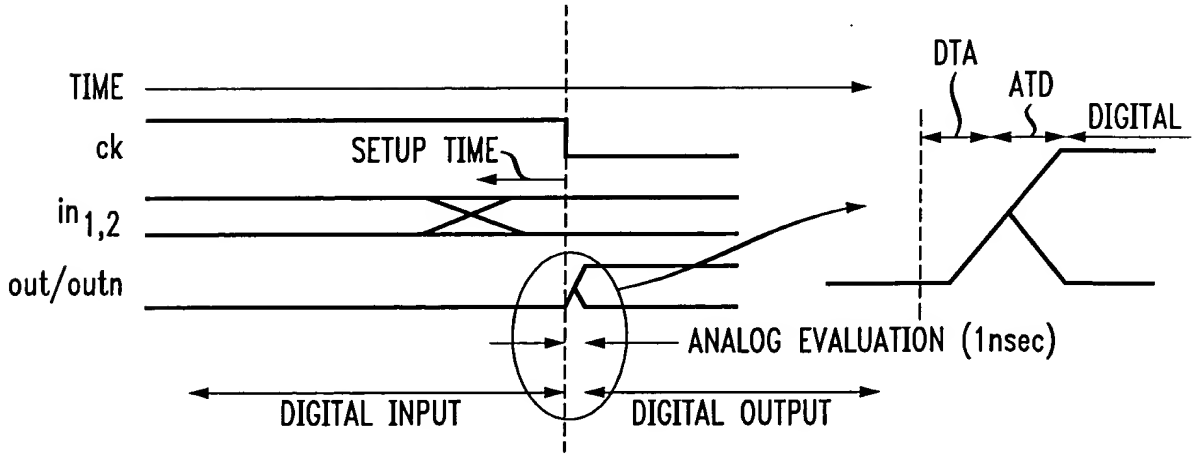

TIME
ck
SETUP TIME
in1,2
out/outn
DTA
ATD
DIGITAL
ANALOG EVALUATION (1nsec)
DIGITAL INPUT
DIGITAL OUTPUT

FIG. 13

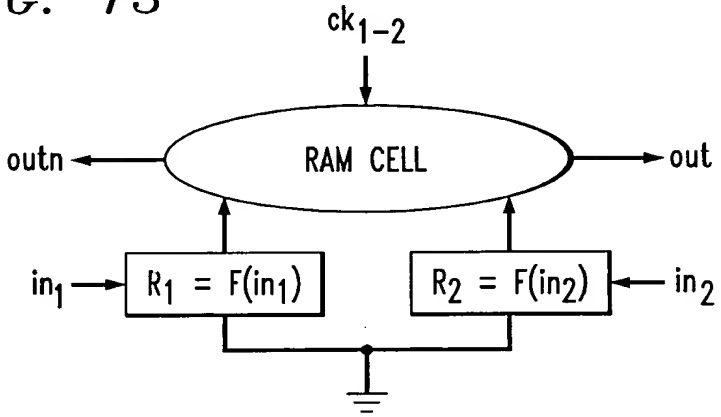


FIG. 14

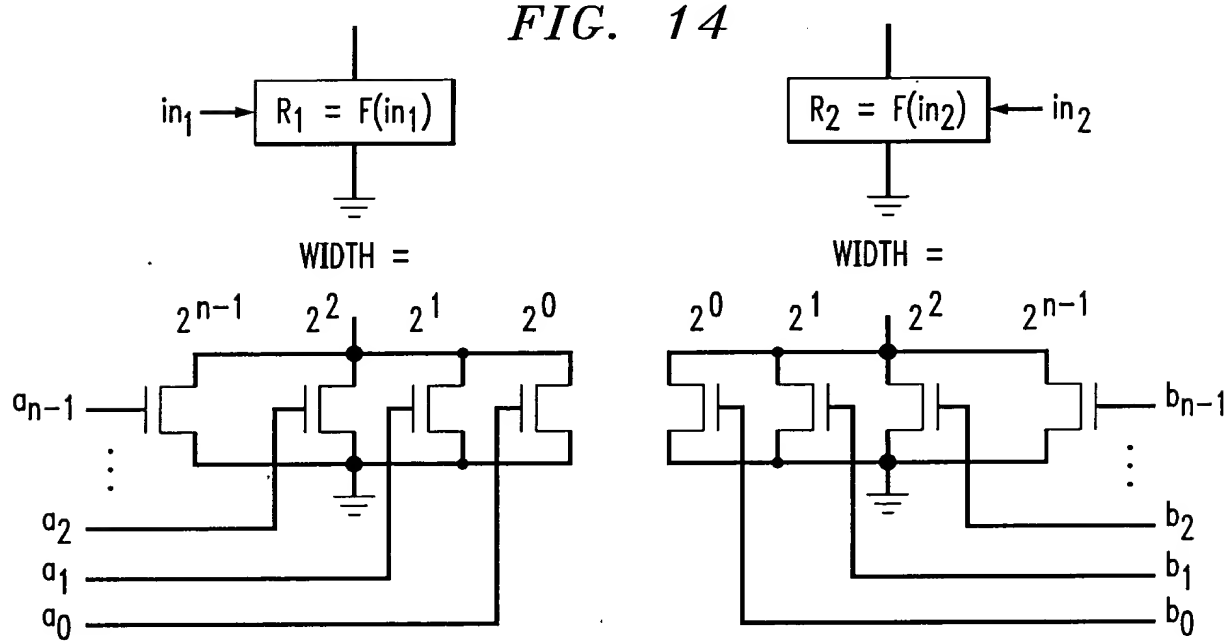


FIG. 15

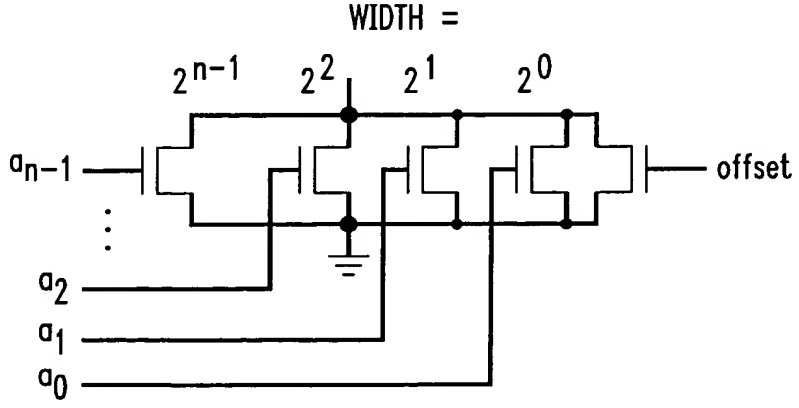


FIG. 16

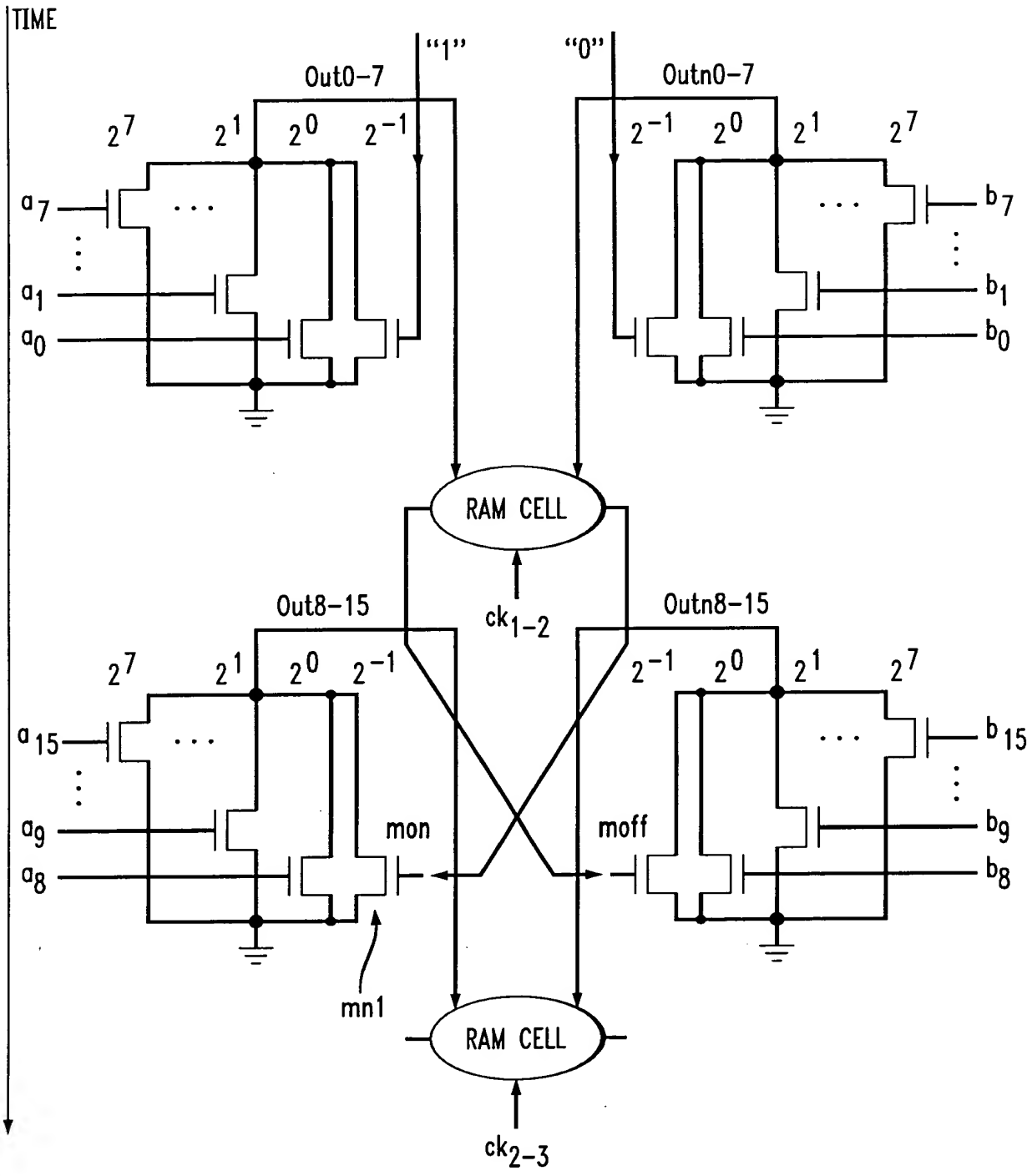

TIME
"1"
"0"
Out0-7
Outn0-7
2^7
2^1
2^0
2^{-1}
a_7
a_1
a_0
b_7
b_1
b_0
RAM CELL
ck_{1-2}
Out8-15
Outn8-15
a_{15}
a_9
a_8
b_{15}
b_9
b_8
mon
moff
mn1
RAM CELL
ck_{2-3}

FIG. 17

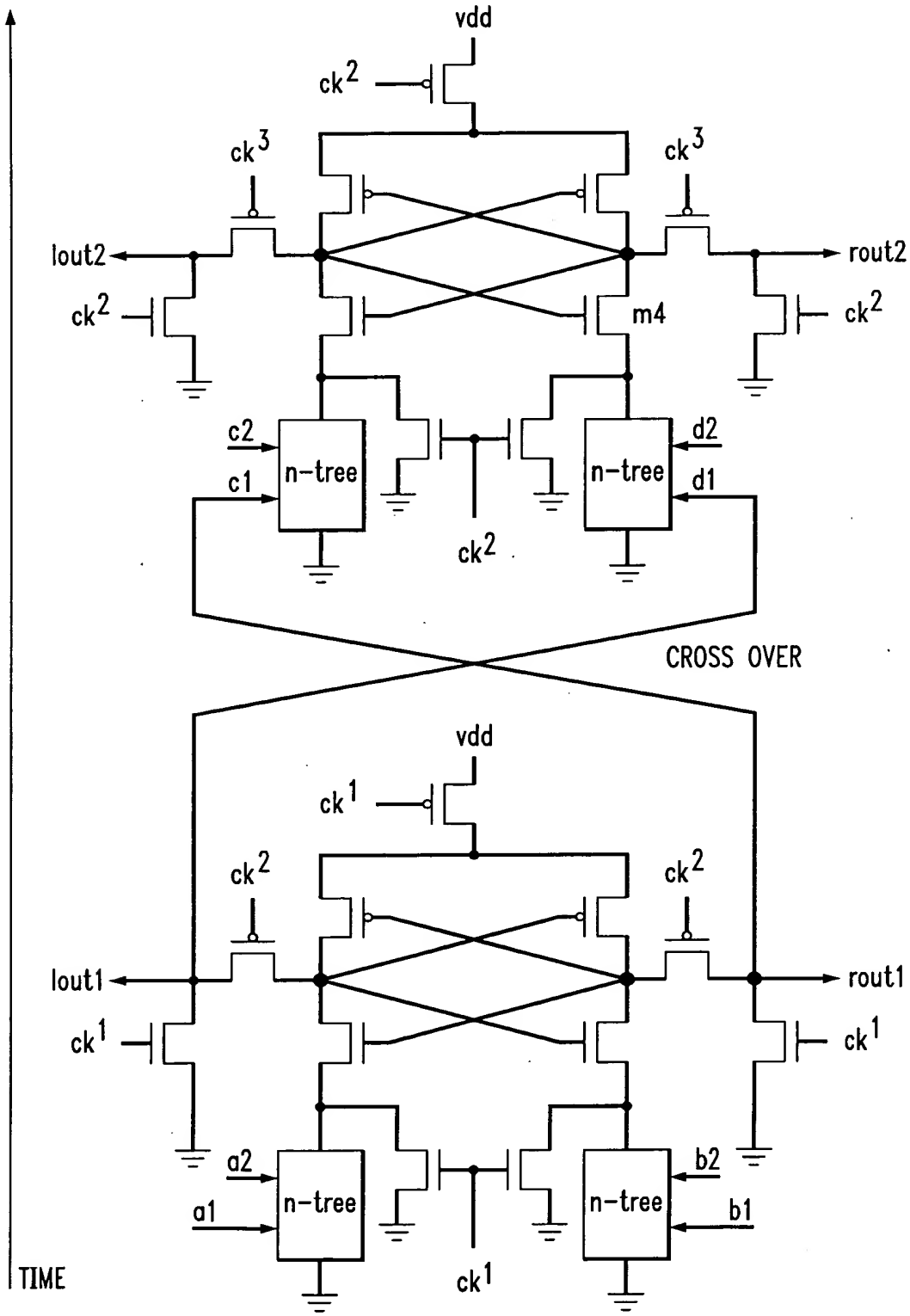

vdd
ck2
ck3
ck3
lout2
rout2
ck2
m4
ck2
c2
d2
c1
n-tree
n-tree
d1
ck2
CROSS OVER
vdd
ck1
ck2
ck2
lout1
rout1
ck1
ck1
a2
b2
a1
n-tree
n-tree
b1
ck1
TIME

FIG. 17 (CONT'D)

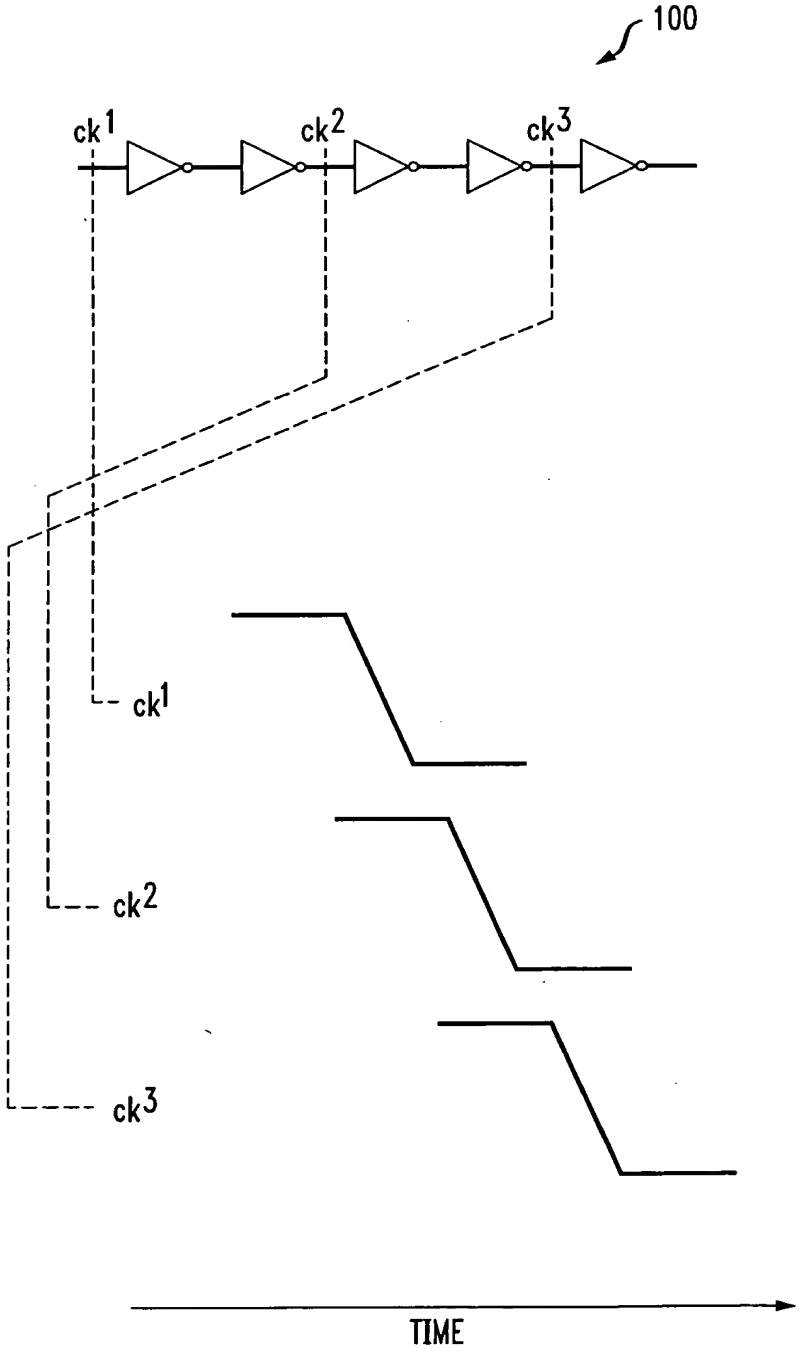


FIG. 18

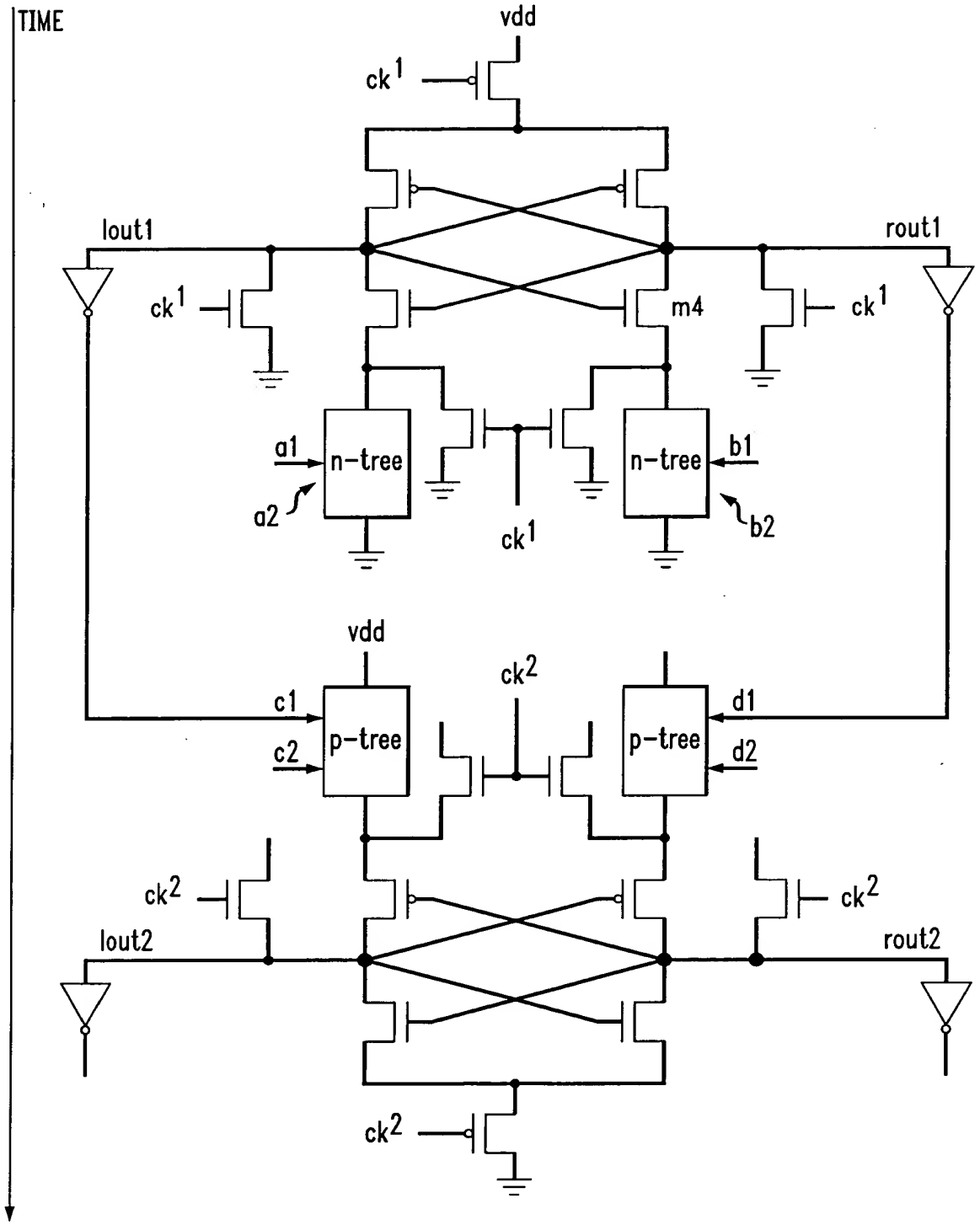

TIME
vdd
ck1
lout1
rout1
ck1
m4
ck1
a1
n-tree
b1
n-tree
a2
ck1
b2
vdd
ck2
c1
p-tree
d1
p-tree
c2
d2
ck2
ck2
lout2
rout2
ck2

FIG. 18 (CONT'D)

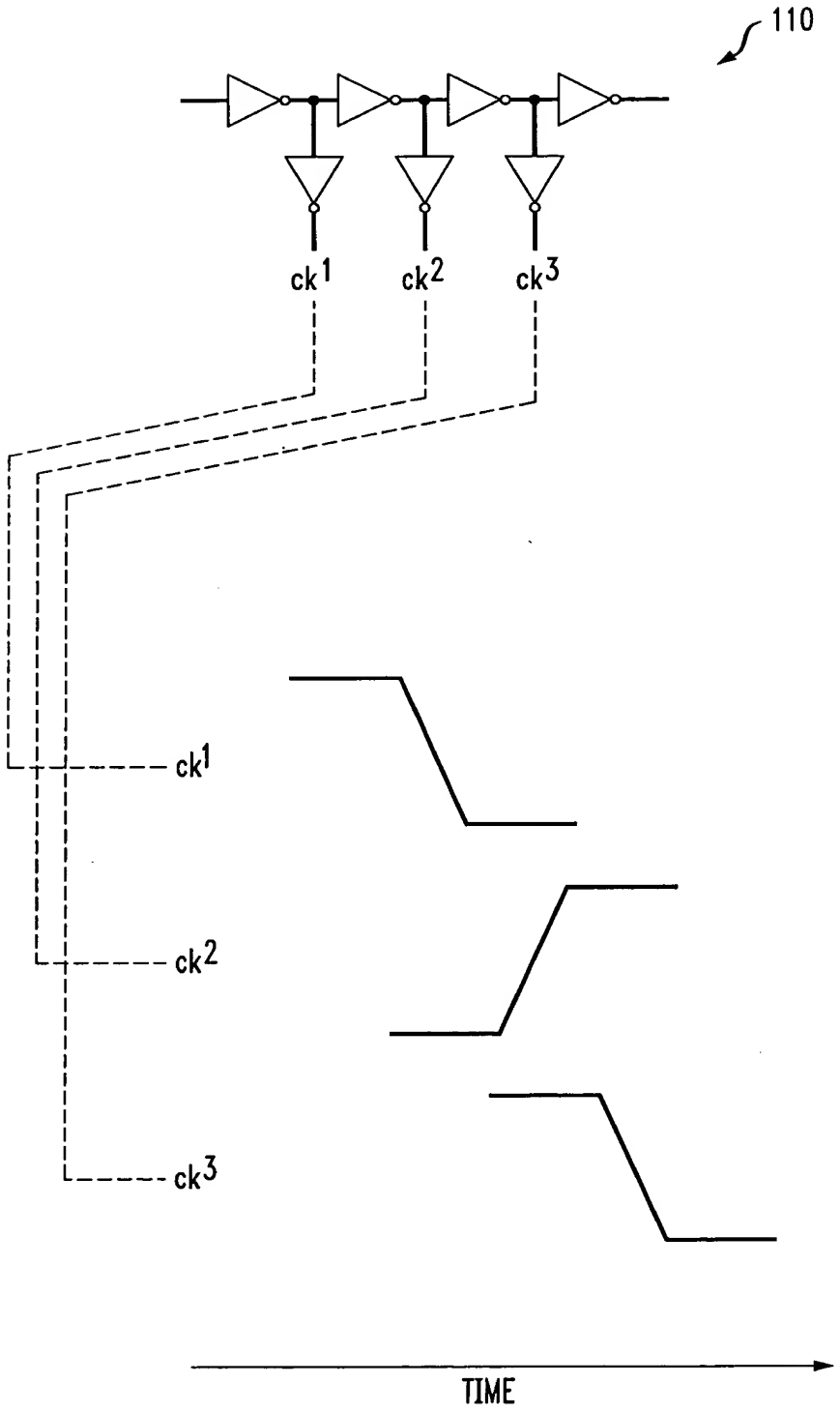


FIG. 19

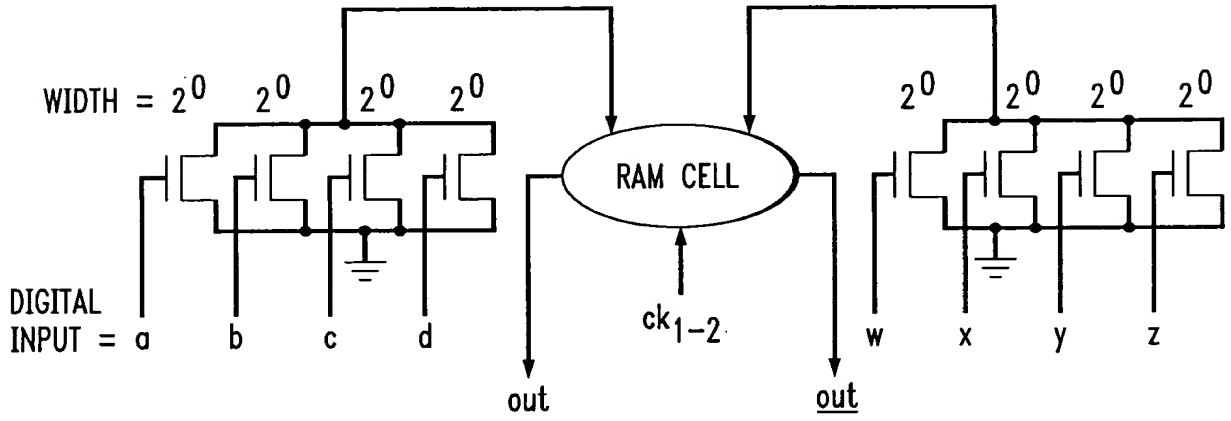

WIDTH = 2^0 2^0 2^0 2^0
2^0 2^0 2^0 2^0
RAM CELL
DIGITAL INPUT = a b c d
ck_{1-2}
w x y z
out
out

FIG. 20

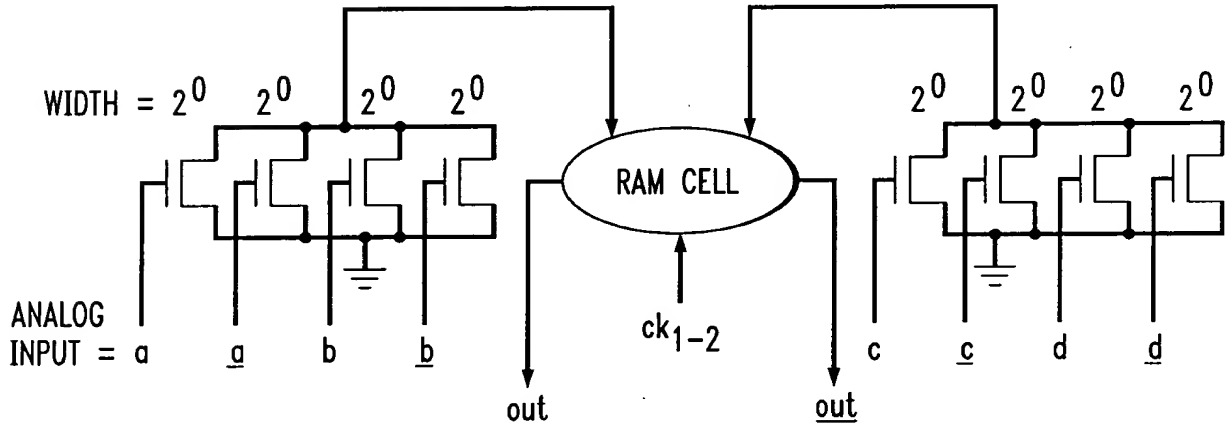

WIDTH = 2^0 2^0 2^0 2^0
2^0 2^0 2^0 2^0
RAM CELL
ANALOG INPUT = a $\underline{a}$ b $\underline{b}$
ck_{1-2}
c $\underline{c}$ d $\underline{d}$
out
out

FIG. 21

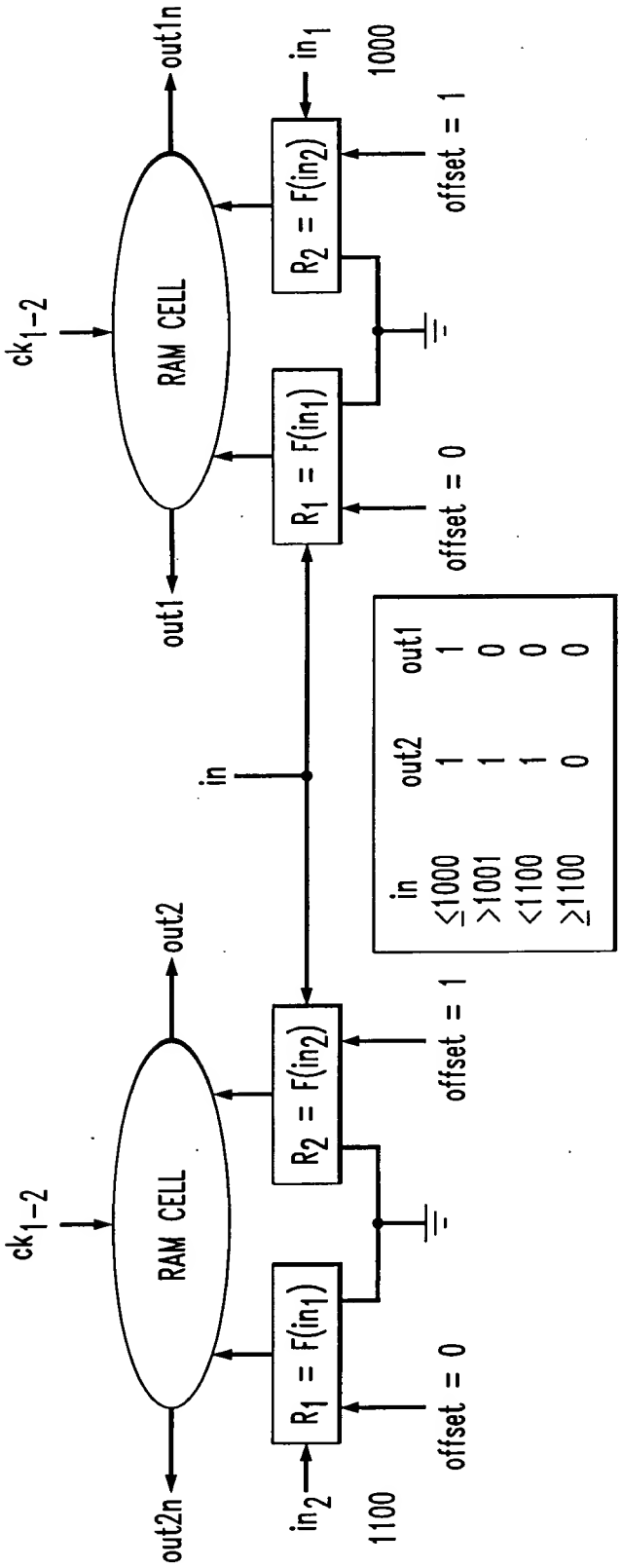

out1n
out1
out2
out2n
RAM CELL
RAM CELL
ck1-2
ck1-2
in1
in2
1000
1100
R2 = F(in2)
R1 = F(in1)
R2 = F(in2)
R1 = F(in1)
offset = 1
offset = 0
offset = 1
offset = 0
in
in out2 out1
≤1000 1 1
>1001 1 0
<1100 1 0
≥1100 0 0

FIG. 22

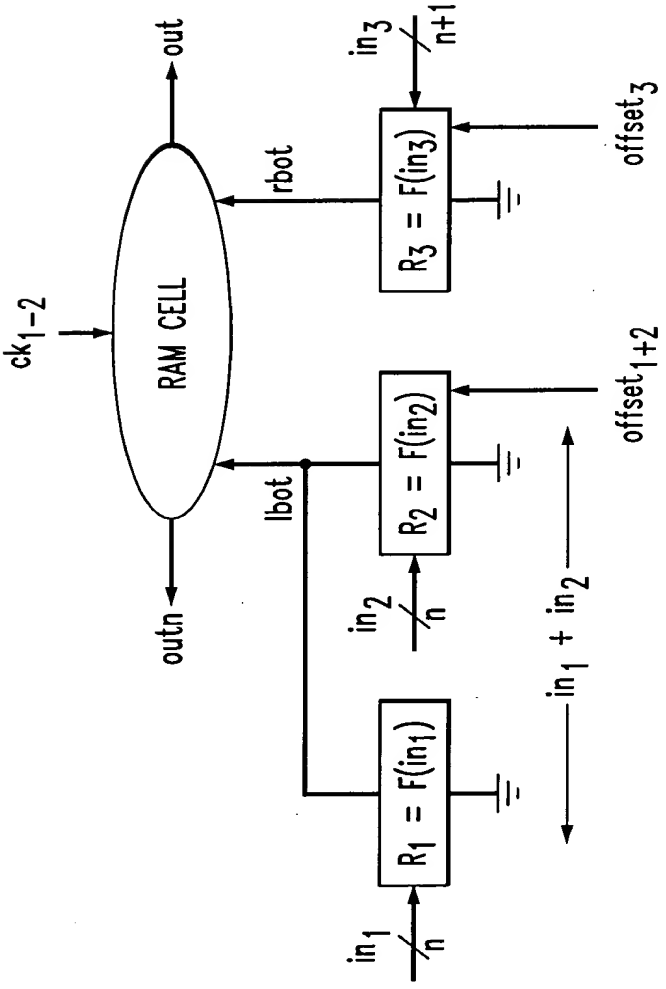

out
in3
n+1
offset3
rbot
R3 = F(in3)
ck1-2
RAM CELL
offset1+2
lbot
R2 = F(in2)
outn
in2
n
in1 + in2
R1 = F(in1)
in1
n

FIG. 23

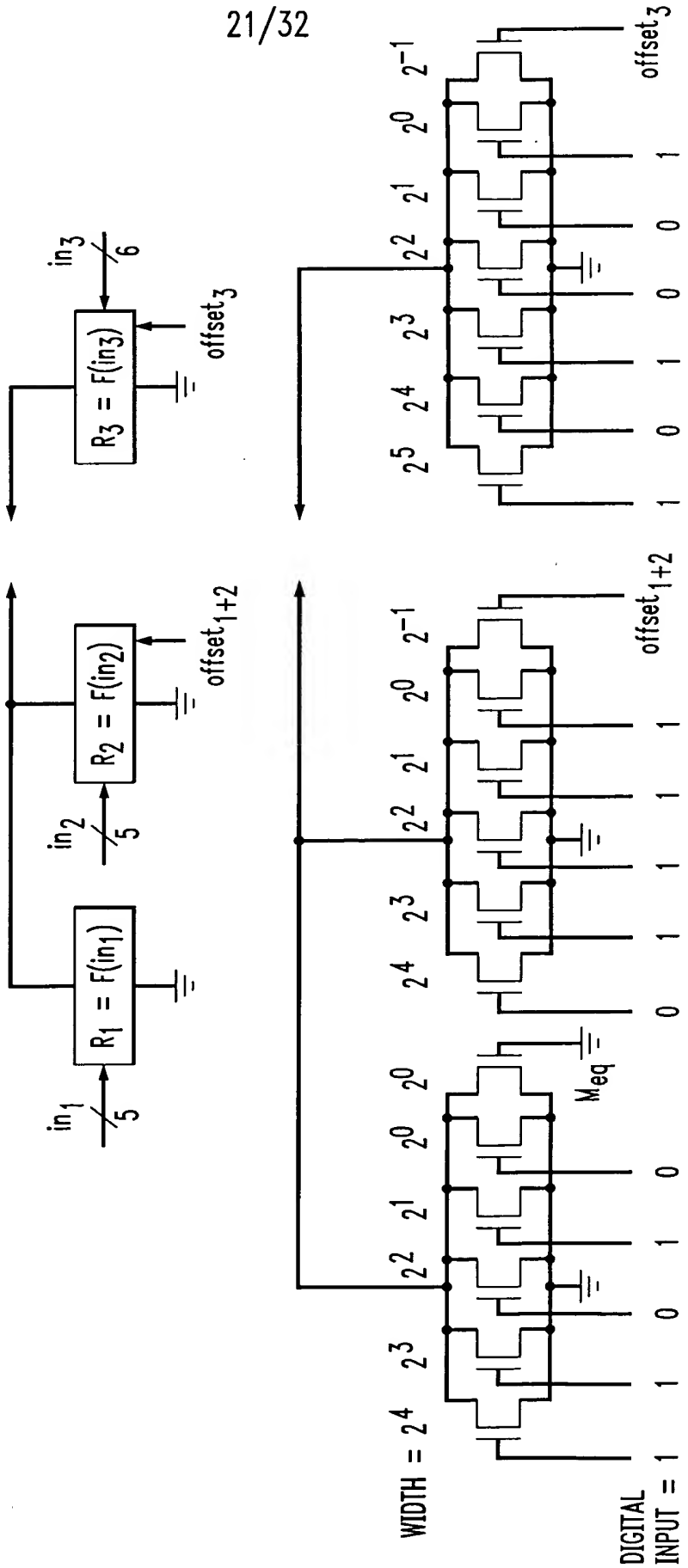
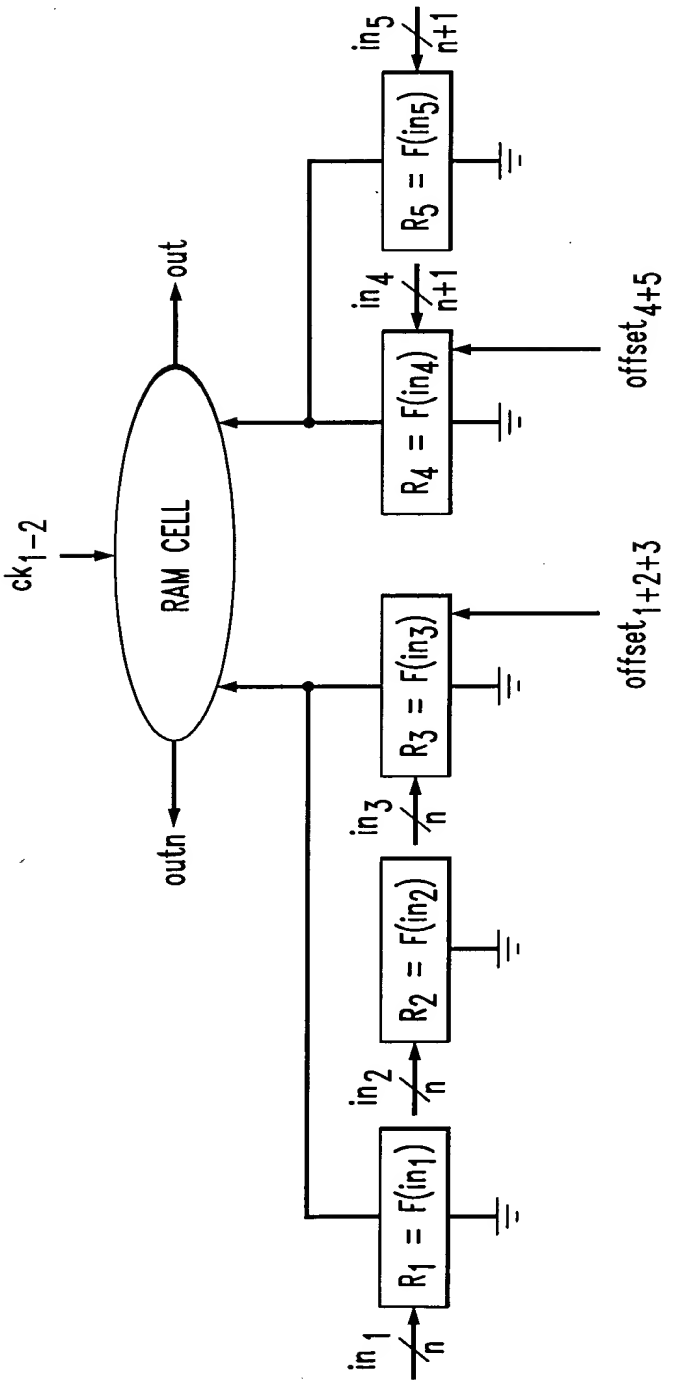

in1
5
R1 = F(in1)
in2
5
R2 = F(in2)
offset1+2
in3
6
R3 = F(in3)
offset3
WIDTH = 2^4
DIGITAL INPUT = 1
Meq
offset1+2
offset3

FIG. 24A


RAM CELL
ck1-2
out
outn
in1
in2
in3
in4
in5
n
n+1
R1 = F(in1)
R2 = F(in2)
R3 = F(in3)
R4 = F(in4)
R5 = F(in5)
offset1+2+3
offset4+5

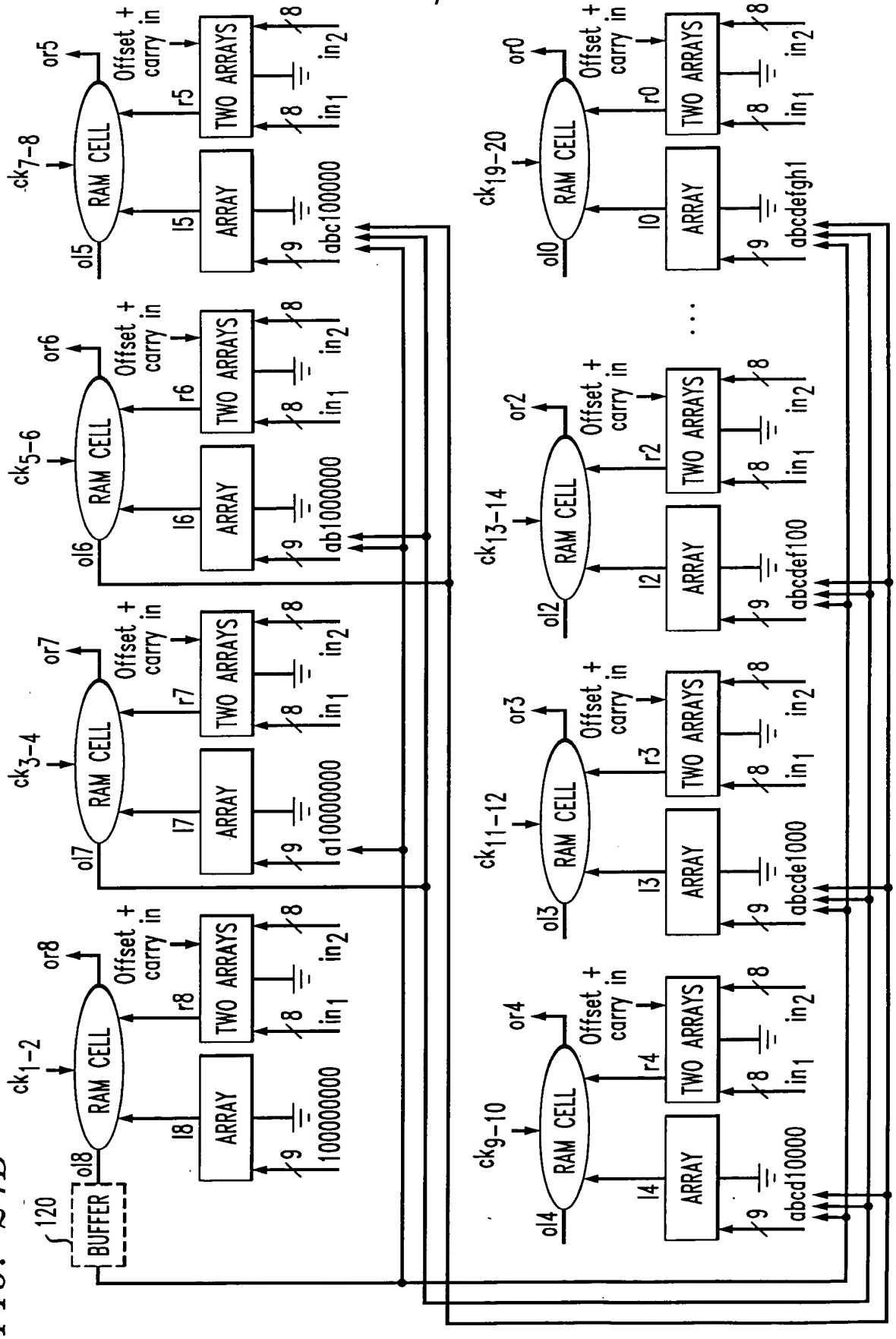

BUFFER
120
RAM CELL
ARRAY
TWO ARRAYS
Offset + carry in
100000000
a1000000
ab1000000
abc100000
abcd10000
abcde1000
abcdef100
abcdefgh1

FIG. 24B

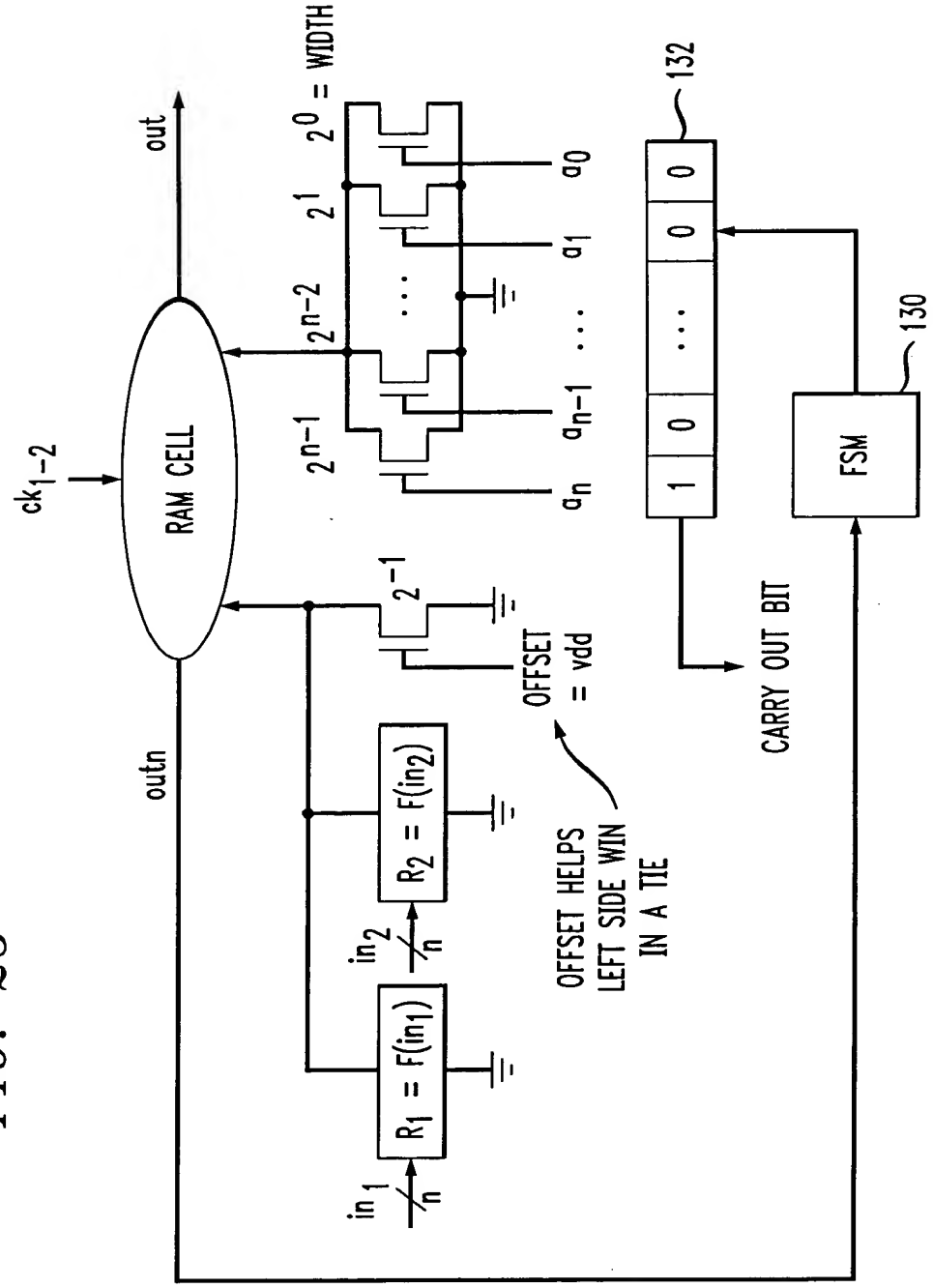

out
outn
RAM CELL
ck1-2
2^0 = WIDTH
2^1
2^n-2
2^n-1
a0
a1
an-1
an
2^-1
OFFSET
= vdd
OFFSET HELPS
LEFT SIDE WIN
IN A TIE
R1 = F(in1)
R2 = F(in2)
in1
in2
n
132
1
0
0
0
CARRY OUT BIT
FSM
130

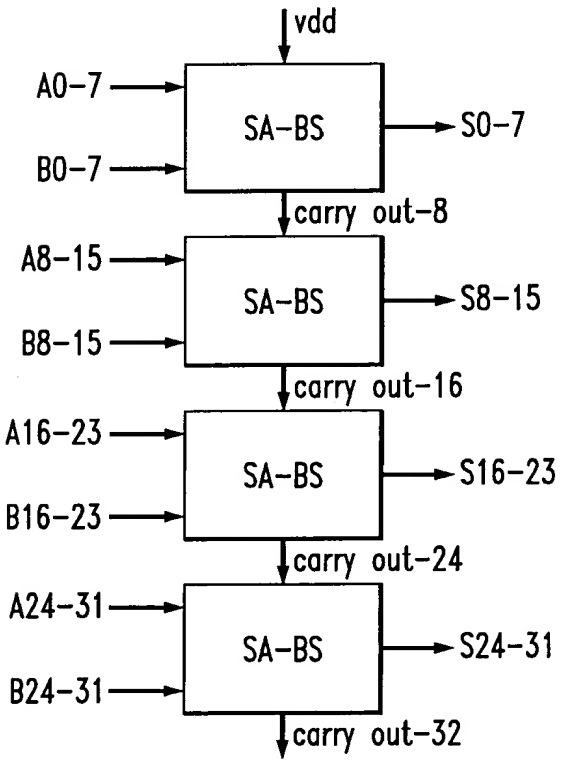
FIG. 25

FIG. 26

```
/* initialize */
n=8 ;
a[n] = 1;
for (k=1; k<n; k++)
   a[k]=0;

for (i=0; i<n; ++i) /* i=clock tick*/
  if (out = 0)
     a[n-i-1] = 1;
  else {
     a[n-i] = 0;
       if (i < n - 1)
          a[n-i-1] = 1;
  }
/* addition result is in array a[n] */
```

FIG. 27



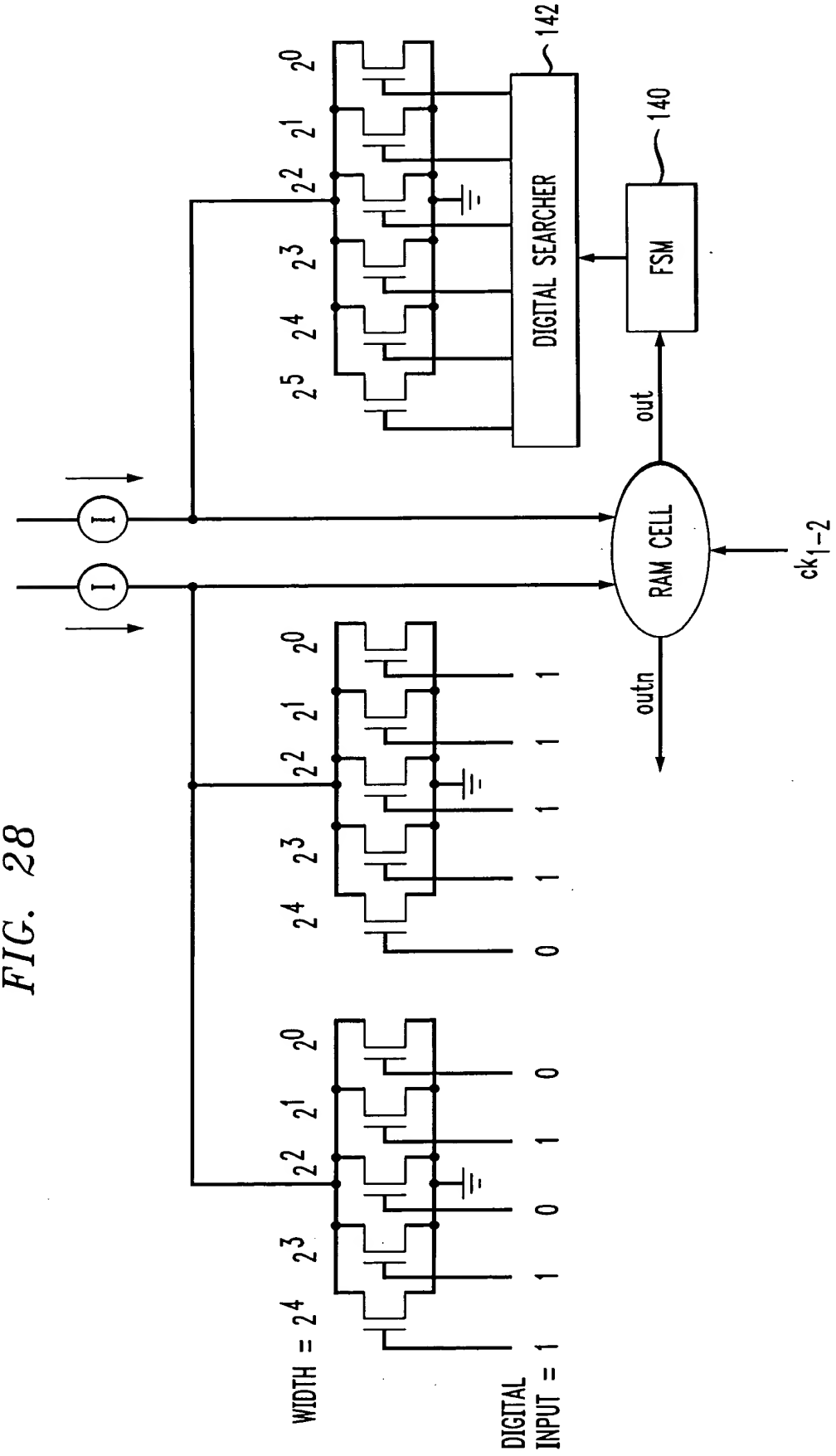

142
140
DIGITAL SEARCHER
FSM
out
outn
RAM CELL
ck_{1-2}
I
I
2^0
2^1
2^2
2^3
2^4
2^5
WIDTH = 2^4
DIGITAL INPUT = 1 1 0 1 0
0 1 1 1 1
1 1 1 1 1

FIG. 28

FIG. 29

PRIOR ART

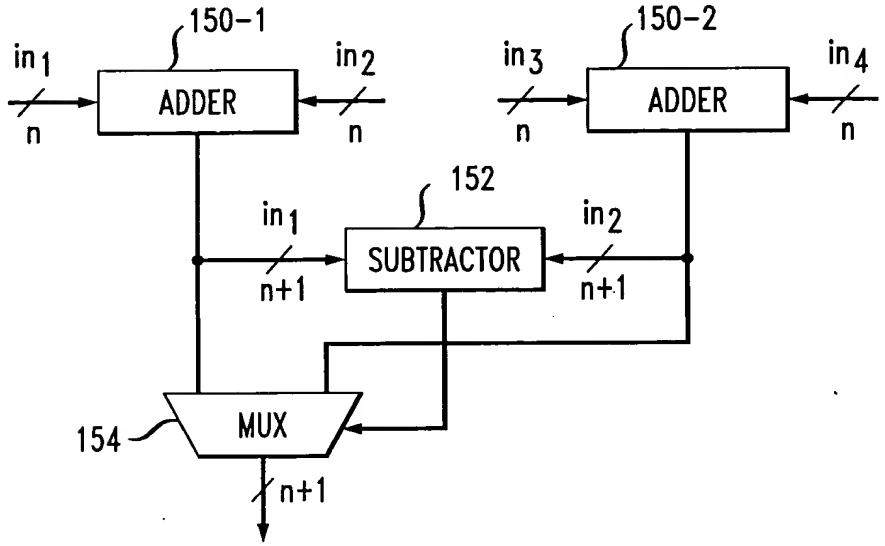


FIG. 30

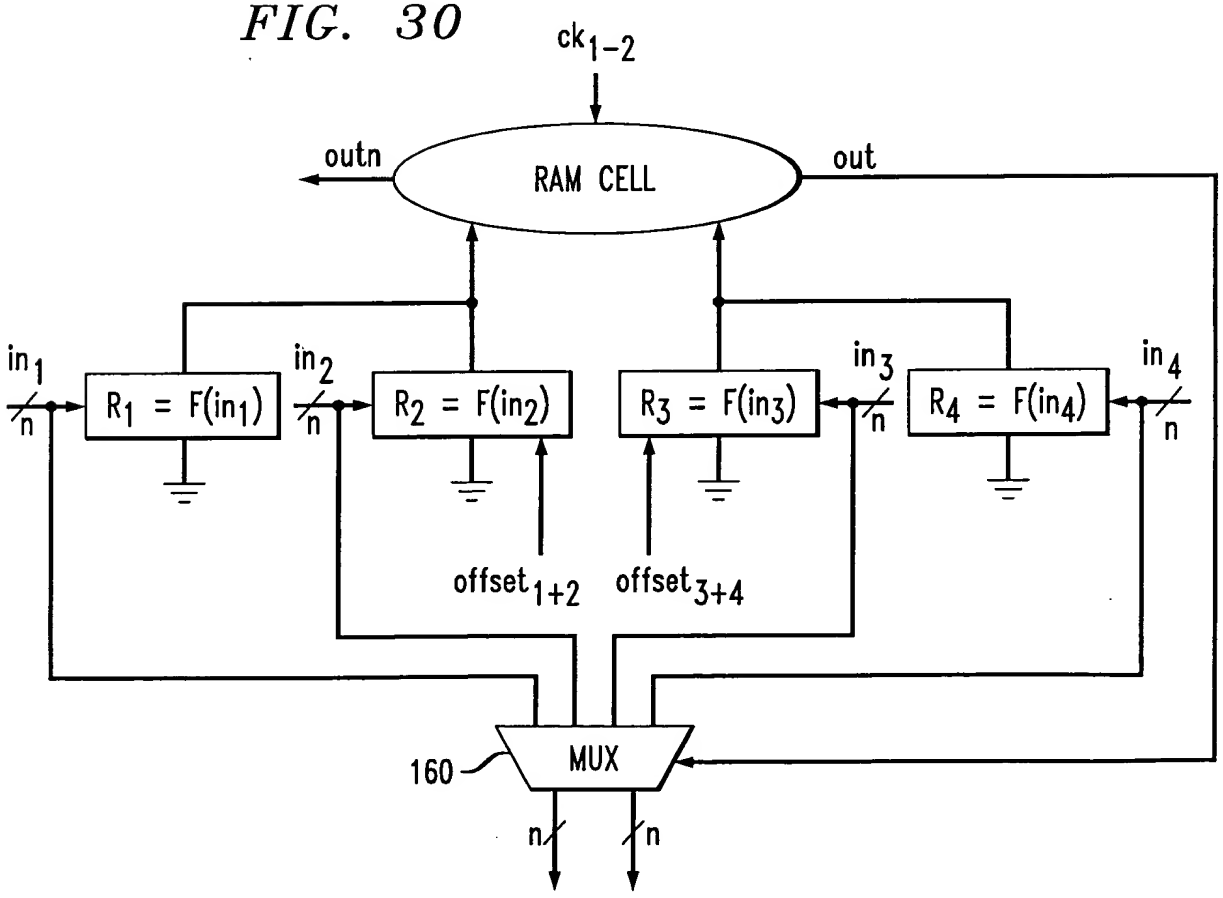


FIG. 31

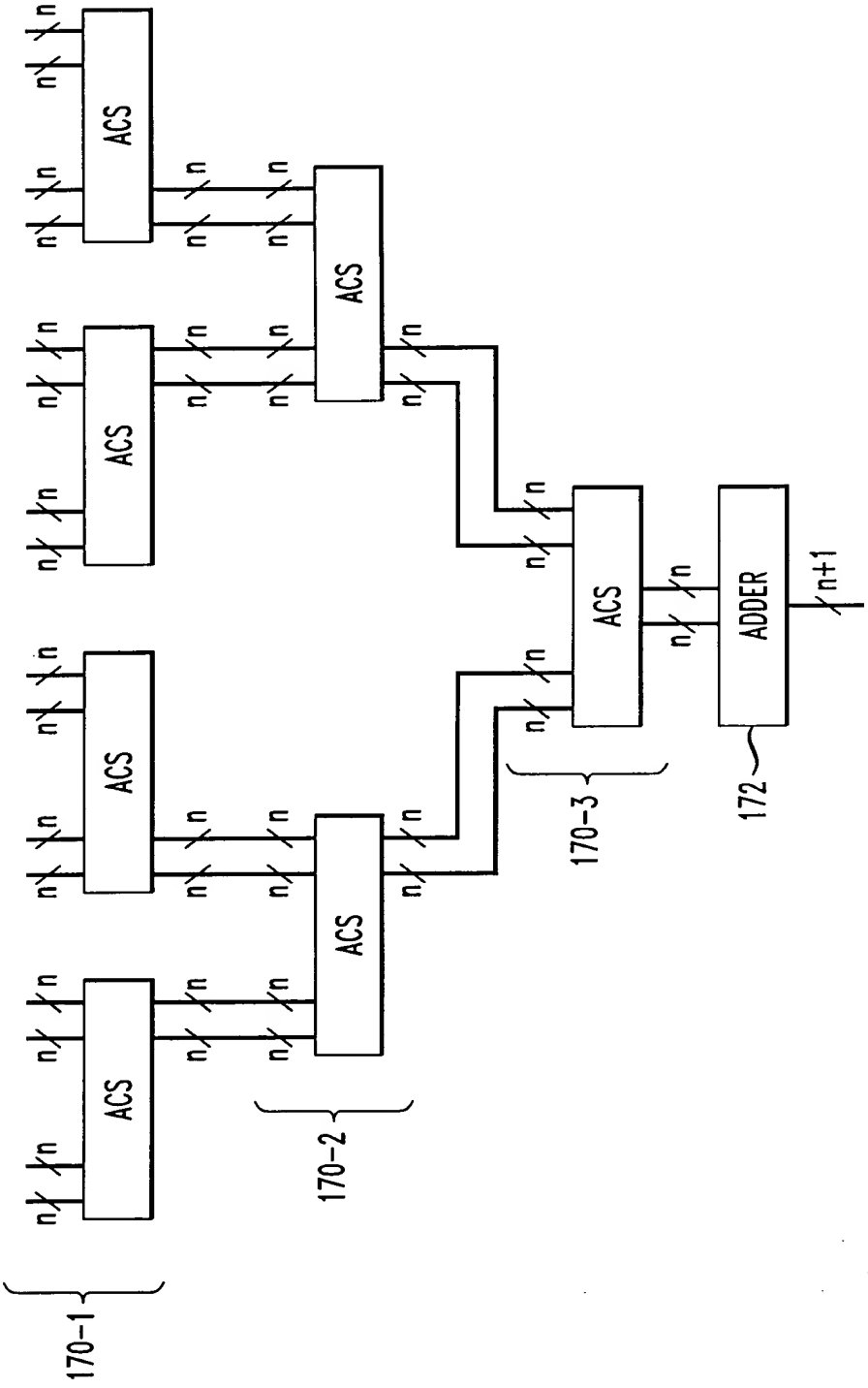


FIG. 32

	POWER (μW)		TRANSISTOR COUNT		DELAY (pSEC)	
	ADD COMPARE	SELECT	ADD COMPARE	SELECT	ADD COMPARE	SELECT
CONVENTIONAL	2000	200	5215	58	1120	200
SEESAW	100	300	55	108	516	173
GAIN FACTOR	X20	X0.66	X95	X0.54	X2.17	X1.15

FIG. 33

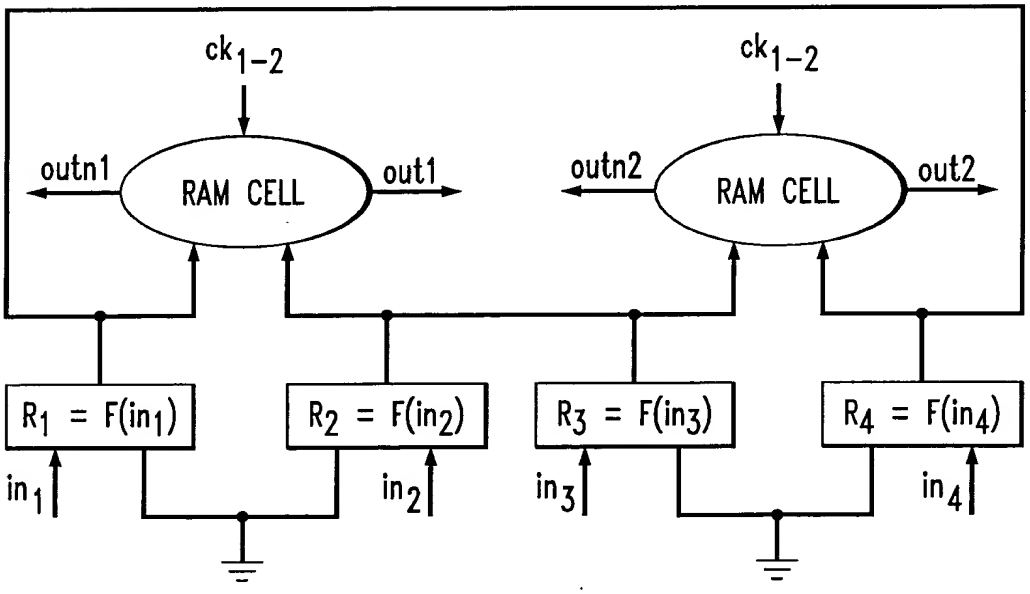
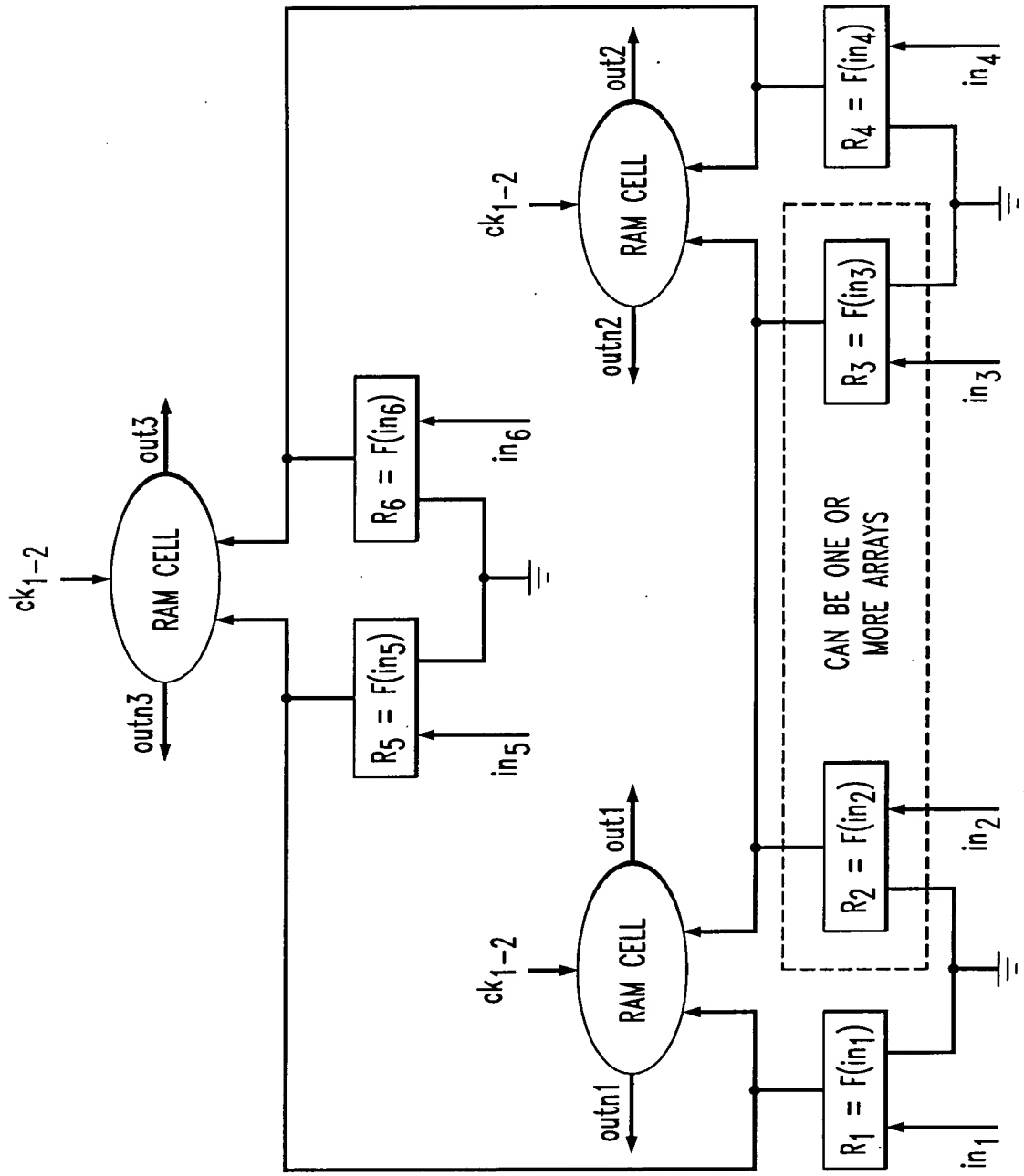


FIG. 34


RAM CELL
ck1-2
out1
outn1
out2
outn2
out3
outn3
R1 = F(in1)
R2 = F(in2)
R3 = F(in3)
R4 = F(in4)
R5 = F(in5)
R6 = F(in6)
in1
in2
in3
in4
in5
in6
CAN BE ONE OR MORE ARRAYS

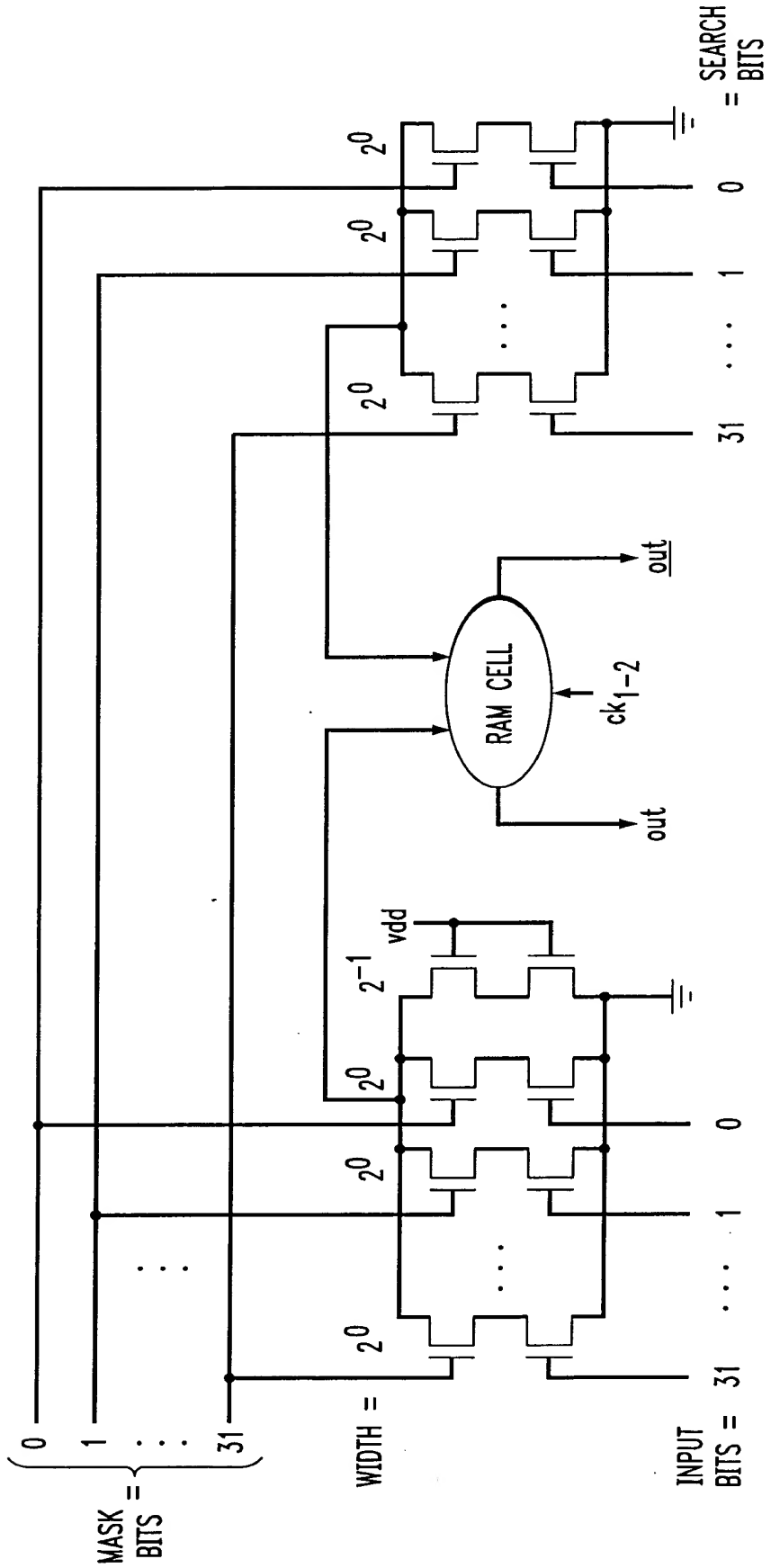
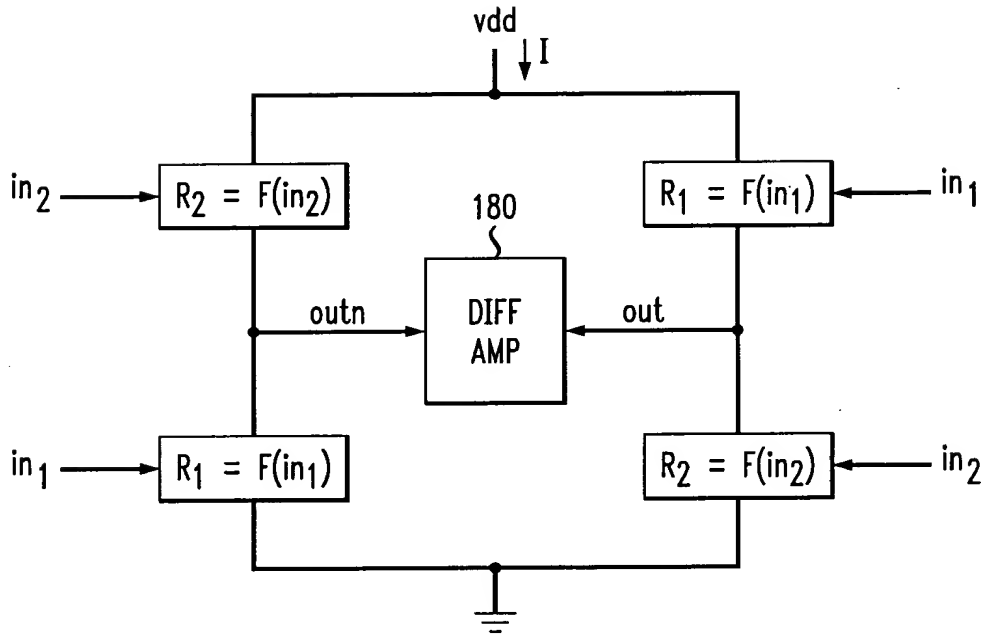

SEARCH BITS = 0
1
31
2^0
RAM CELL
ck_{1-2}
out
out
vdd
2^{-1}
WIDTH =
INPUT BITS = 31 ... 1 0
MASK BITS = 0 1 ... 31

FIG. 35

FIG. 36


vdd
I
in2
R2 = F(in2)
180
R1 = F(in1)
in1
outn
DIFF
AMP
out
in1
R1 = F(in1)
R2 = F(in2)
in2